MOHAN BABU UNIVERSITY

Sree Sainath Nagar, Tirupati – 517 102

MBU
MOHAN BABU
UNIVERSITY
DREAM. BELIEVE. ACHIEVE

SCHOOL OF ENGINEERING

M.Tech. VLSI and Embedded System Design

CURRICULUM AND SYLLABUS

(From 2022-23 Admitted Batches)

FULLY FLEXIBLE CHOICE BASED CREDIT SYSTEM (FFCBCS)

MOHAN BABU UNIVERSITY

Vision

To rise as one of the greatest hubs of innovation and entrepreneurship in the country, wherein students empower themselves with the best of knowledge, unleash their potential to the fullest, and soar high to attain a brighter future for themselves and the nation.

Mission

- To provide relevant knowledge founded on the spirit of curiosity, compassion, courage and commitment.
- To uphold novelle wings of leadership and excellence under expert mentors who guide students towards wisdom and knowledge.
- To create a dynamic learning environment that empowers learners with the right blend of passion and purpose to build a glorious tomorrow.

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

VISION

To be a center of excellence in the fields of Electronics, Communications and Instrumentation through teaching and research producing high quality engineering professionals and Entrepreneurs with values and ethics to meet local and global demands.

MISSION

- Imparting knowledge through contemporary curriculum and striving for development of students with diverse background.
- Developing skills for enhancing employability of students through comprehensive training process.
- Inspiring students and faculty members for innovative research through constant interaction with research organizations and industry to meet societal needs.
- Inculcating ethics and values in students for effective engineering practice.

M.Tech. VLSI AND EMBEDDED SYSTEM DESIGN

PROGRAM EDUCATIONAL OBJECTIVES

After few years of graduation, the graduates of M. Tech. (VLSI & Embedded Systems Design) Program would have

PEO1. Pursued research studies in the core or allied areas.

PEO2. Successful entrepreneurial or technical career in the core or allied areas of VLSI and Embedded systems

PEO3. Continued to learn and to adapt evolving technologies in the core or allied areas of VLSI and Embedded systems.

PROGRAM OUTCOMES

On successful completion of the Program, the graduates of M. Tech. (VLSI & Embedded Systems Design) will be able to:

PO1. Demonstrate mastery of knowledge in VLSI, Embedded Systems and other allied areas of the program.

PO2. Design and develop Integrated Circuits/systems for Digital and Mixed signal applications using advanced Microcontroller based systems and FPGA/ASICs.

PO3. Select and apply appropriate modern tools, techniques and resources to provide engineering solutions in VLSI and Embedded Systems.

PO4. Independently carry out research to deliver solutions for complex problems in the area of VLSI and Embedded Systems.

PO5. Communicate effectively in written and oral formats.

PO6. Ability to continuously engage in life-long learning to enhance knowledge and competence.

M.Tech. VLSI and Embedded System Design

Basket Wise - Credit Distribution

S. No.	Basket	Credits (Min.- Max.)
1	SCHOOL CORE	31-34
2	PROGRAM CORE	21-24
3	PROGRAM ELECTIVE	12-18
5	UNIVERSITY ELECTIVE	6
	TOTAL CREDITS	**Min. 70**

School Core (31-34 Credits)

Course Code	Title of the Course	Lecture	Tutorial	Practical	Project based Learning	Credits	Pre-requisite
		L	T	P	S	C	
22EC201001	Computational Methods in Microelectronics	3	-	-	-	3	-
22EE201001	Research Methodology	3	-	-	-	3	-
22EE201002	Innovations and Intellectual Property Rights	2	-	-	-	2	-
22EC211001	Internship	-	-	-	-	2	-
22EC209001	Project Work Phase-I	-	-	-	-	10	-
22EC210001	Project Work Phase-II	-	-	-	-	14	-
Mandatory Courses (Min. 4 Credits) Earned Credits will not be considered for CGPA							
22AI207601	Statistics with R	2	-	-	-	2	-
22LG207601	Technical Report Writing	2	-	-	-	2	-
22MG207601	Project Management	2	-	-	-	2	-
22MG207602	Essentials of Business Etiquettes	2	-	-	-	2	-

Program Core (21-24 Credits)

Course Code	Title of the Course	Lecture	Tutorial	Practical	Project based Learning	Credits	Pre-requisite
		L	T	P	S	C	
22EC202002	Analog CMOS VLSI Design	3	-	3	-	4.5	-
22EC202003	Digital CMOS VLSI Design	3	-	3	-	4.5	-
22EC202004	VLSI Design Verification and Testing	3	-	3	-	4.5	-
22EC201005	Device Modeling	3	-	-	-	3	-
22EC201006	Advanced Computer Architecture	3	-	-	-	3	-
22EC202007	Embedded Systems Design	3	-	3	-	4.5	-

Program Elective (12-18 Credits)

Course Code	Knowledge Area	Title of the Course	Lecture	Tutorial	Practical	Project based Learning	Credits	Pre-requisite
			L	T	P	S	C	
22EC201008	Digital VLSI	Network-on-Chip Design	3	-	-	-	3	Co Design, System-on-Chip Design
22EC201009		IC Fabrication	3	-	-	-	3	-
22EC202010		Nano Materials and Nanotechnology	3	-	3	-	4.5	IC Fabrication
22EC202011		Low Power CMOS VLSI Design	3	-	3	-	4.5	Digital CMOS VLSI Design
22EC201012	Mixed VLSI	CMOS RF Circuit Design	3	-	-	-	3	Analog CMOS VLSI Design
22EC201013		System-on-Chip Design	3	-	-	-	3	Digital CMOS VLSI Design
22EC202014		Mixed Signal Design	3	-	3	-	4.5	-

Course Code	Knowledge Area	Title of the Course	Lecture	Tutorial	Practical	Project based Learning	Credits	Pre-requisite
			L	T	P	S	C	
22EC202015		FPGA Architectures	3	-	3	-	4.5	-
22EC201016		Physical Design Automation	3	-	_	-	3	Digital CMOS VLSI Design, FPGA Architectures
22EC202017		Memory Technologies	3	-	3	-	4.5	Digital CMOS VLSI Design, IC Fabrication, VLSI Design Verification and Testing
22EC203018		Reconfigurable Computing	3	-	-	4	4	FPGA Architectures
22EC203019		VLSI Digital Signal Processing	3	-	-	4	4	Computational Methods in Microelectronics
22EC201020	Embedded Systems	Electromagnetic Interference and Compatibility	3	-	_	-	3	-
22EC201021		Fault Tolerant and Dependable Systems	3	-	_	-	3	-
22EC201022		Communication Buses and Interfaces	3	-	-	-	3	Embedded Systems Design
22EC201023		Co Design	3	-	-	-	3	-
22EC202024		Real Time Systems	3	-	3	-	4.5	Embedded Systems Design
22EC203025		Advanced Embedded Systems	3	-	-	4	4	Embedded Systems Design

University Elective (6 Credits)

Course Code	Title of the Course	Lecture	Tutorial	Practical	Project based Learning	Credits
		L	T	P	S	C
22AI201701	Business Analytics	3	-	-	-	3
22CM201701	Cost Management of Engineering Projects	3	-	-	-	3
22CE201701	Disaster Management	3	-	-	-	3
22SS201701	Value Education	3	-	-	-	3
22SS201702	Pedagogy Studies	3	-	-	-	3
22LG201701	Personality Development through Life Enlightenment Skills	3	-	-	-	3

Note:

1. If any student has chosen a course or equivalent course from the above list in their regular curriculum then, he/she is not eligible to opt the same course/s under University Elective.
2. The student can choose courses from other disciplines offered across the schools of MBU satisfying the pre-requisite other than the above list.

SCHOOL CORE

Course Code	Course Title	L	T	P	S	C
22EC201001	COMPUTATIONAL METHODS IN MICROELECTRONICS	3	-	-	-	3

Pre-Requisite -

Anti-Requisite -

Co-Requisite -

COURSE DESCRIPTION: This course provides a detailed discussion on Linear and Nonlinear Systems - modelling, Approximation, Interpolation, Curve Fitting, Numerical Integration, Finite Difference Techniques, Initial Value problems, Finite Element Methods, Method of Characteristics, Finite Volume Methods, Grid Generation and Error Estimation, Device and Process Simulation, Layout and Yield estimation algorithms, Symbolic analysis and Synthesis of Analog ICs.

COURSE OUTCOMES: After successful completion of the course, students will be able to:

CO1. Apply Approximation, Interpolation, Curve Fitting and Numerical Integration to obtain accuracy in Linear and Non-linear Systems.

CO2. Analyze numerical solutions of partial differential equations to evaluate the performance of structural designs modelled in computational tools for multidisciplinary applications.

CO3. Apply grid generation and refinement algorithms to reduce the error in estimation of initial and final value problems of computational tools.

CO4. Apply device and process simulation to perform synthesis of Analog ICs at various levels of abstraction for improving yield.

CO-PO Mapping Table:

Course Outcomes	Program Outcomes					
	PO1	PO2	PO3	PO4	PO5	PO6
CO1	3	3	3	-	-	-
CO2	3	3	3	-	-	-
CO3	3	3	3	-	-	-
CO4	3	3	3	-	-	-
Course Correlation Mapping	**3**	**3**	**3**	**-**	**-**	**-**

Correlation Levels: 3: High; 2: Medium; 1: Low

COURSE CONTENT

Module 1: BASIC COMPUTATION TOOLS ***(12 Periods)***

Linear Systems and Matrices – Matrix Formalities, Condition of Matrix Systems, Techniques for Matrix Solution, Mixed Boundary Condition. Nonlinear Systems – Scalar Equations, Matrix Equations. Approximation, Interpolation, Curve Fitting, Numerical Integration.

Module 2: COMPUTATIONAL TOOLS - I ***(07 Periods)***

Finite Difference Techniques, Initial Value Problems, Finite Element Methods.

Module 3: COMPUTATIONAL TOOLS - II ***(07 Periods)***

Method of Characteristics – Classification of Partial Differential Equations, Investigations in Engineering, Finite volume Methods – Direct Analysis.

Module 4: GRID GENERATION AND ERROR ESTIMATES ***(10 Periods)***

Grid generation, Triangulation, errors and mesh Selection, Refinement Algorithms, Mesh Redistribution, Moving Grids.

Module 5: APPLICATIONS TO DEVICE AND PROCESS SIMULATION ***(09 Periods)***

Applications to device and process simulation, Layout algorithms, Yield estimation algorithms, Symbolic analysis and Synthesis of Analog ICs.

Total Periods: 45

EXPERIENTIAL LEARNING

1. Develop a CMOS circuit and extract the related parameters using VLSI based CAD Tool.
2. Simulate layout algorithms in a VLSI based CAD Tool.
3. Optimize the layout for various goals like area, delay and power.

RESOURCES

TEXT BOOKS:

1. Herbert Koenig, "Modern Computational methods", CRC Press, 1988.
2. Graham F. Carey, "Computational Grids: generations, adaptation & Solution Strategies", CRC Press, 1997.
3. L.Pallage, R.Rohrer and C.Visweswaraiah, "Electronic Circuit and System Simulation Methods", McGraw Hill, 1995.

REFERENCE BOOKS:

1. Naveed A. Sherwani, "Algorithms for VLSI Physical Design Automation", Springer, 2nd Edition 2012.

VIDEO LECTURES:

1. https://nptel.ac.in/downloads/103106074/
2. https://www.coursebuffet.com/course/805/nptel/computational-techniques-iit-madras

Web Resources:

1. https://math.berkeley.edu/~sethian/level_set.html
2. https://link.springer.com/referenceworkentry/10.1007/978-0-387-09766-4_111
3. https://www.ics.uci.edu/~eppstein/gina/vlsi.html

SCHOOL CORE

Course Code	Course Title	L	T	P	S	C
22EE201001	**RESEARCH METHODOLOGY**	3	-	-	-	3

Pre-Requisite --
Anti-Requisite --
Co-Requisite --

COURSE DESCRIPTION:
The course is developed for the students' to understand the underlying concepts of research methodology and a systematic approach for carrying out research in the domain of interest. The course is emphasised on developing skills to recognise and reflect the strength and limitation of different types of research; formulation of the research hypothesis and its systematic testing methods. The course also emphasises on interpreting the findings and research articulating skills along with the ethics of research.

COURSE OUTCOMES: *After successful completion of the course, students will be able to:*
CO5. Demonstrate the underlying concepts of research methodology, types of research and the systematic research process.
CO6. Demonstrate the philosophy of research design, types of research design and develop skills for a good research design.
CO7. Demonstrate the philosophy of formulation of research problem, methods of data collection, review of literature and formulation of working hypothesis.
CO8. Analyse the data and parametric tests for testing the hypothesis.
CO9. Interpret the findings and research articulating skills along with the ethics of research.

CO-PO Mapping Table:

Course Outcomes	Program Outcomes					
	PO1	PO2	PO3	PO4	PO5	PO6
CO1	-	-	-	3	-	-
CO2	-	-	-	3	-	-
CO3	-	-	-	3	-	-
CO4	-	-	-	3	-	-
CO5	-	-	-	-	3	-
Course Correlation Mapping	**-**	**-**	**-**	**3**	**3**	**-**

Correlation Levels: 3: High; 2: Medium; 1: Low

COURSE CONTENT

Module 1: Introduction to Research Methodology (08 Periods)

Meaning of Research, Objectives of Research, Motivation in Research, Types of Research, Research Approaches, Significance of Research, Research Methods versus Methodology, Research and Scientific Method, Research Process, Criteria of Good Research.

Module 2: Research Design (08 Periods)

Research design—Basic Principles, Need of research design, Features of good design, Important concepts relating to research design, Different research designs, Basic principles of experimental designs, Developing a research plan.

Module 3: Research Formulation (08 Periods)

Defining and formulating the research problem - Selecting the problem - Necessity of defining the problem - Importance of literature review in defining a problem – Data collection – Primary and secondary sources; Critical literature review – Identifying gap areas from literature review; Hypothesis— Types of hypothesis, Development of working hypothesis.

Module 4: Analysis of Data and Hypothesis Testing (14 Periods)

Quantitative Tools: Testing and Significance of Measures of Central Tendency, Dispersion; correlation, Principles of least squares—Regression; Errors-Mean Square error, Mean absolute error, Mena absolute percentage errors.
Testing of Hypothesis: Hypothesis Testing Procedure, Types of errors, Parametric testing (t, z and F), Chi-Square Test as a Test of Goodness of Fit; Normal Distribution- Properties of Normal Distribution; Analysis of Variance.

Module 5: Interpretation and Report Writing (07 Periods)

Interpretation: Meaning of interpretation; Techniques of interpretation; Precautions in Interpretation.
Report Writing –Significance, Different Steps, Layout, Types of reports, Mechanics of Writing a Research Report, Precautions in Writing Reports; Research ethics—Plagiarism, Citation and acknowledgement.

Total Periods: *45*

EXPERIENTIAL LEARNING

1. Should conduct a survey based on a hypothesis, analyze the data collected and draw the inferences from the data.
2. Should review the literature on the given topic and should identify the scope/gaps in the literature and develop a research hypothesis.
3. Should study a case, formulate the hypothesis and identify an appropriate testing technique for the hypothesis.
4. Study an article and submit a report on the inferences and should interpret the findings of the article.

TEXT BOOKS:

2. C.R. Kothari, Research Methodology: Methods and Techniques, New Age International Publishers, 2nd revised edition, New Delhi, 2004.
3. Garg, B.L., Karadia, R., Agarwal, F. and Agarwal, *An introduction to Research Methodology*, RBSA Publishers, 2002.

REFERENCE BOOKS:

2. R. Panneerselvam, Research Methodology, PHI learning Pvt. Ltd., 2009.
3. Singh, Yogesh Kumar. *Fundamental of research methodology and statistics*. New Age International, 2006.

VIDEO LECTURES:

1. https://nptel.ac.in/courses/121106007
2. https://onlinecourses.nptel.ac.in/noc22_ge08/preview
3. https://www.youtube.com/watch?v=VK-rnA3-41c

Web Resources:

1. https://www.scribbr.com/category/methodology/
2. https://leverageedu.com/blog/research-design/
3. https://prothesiswriter.com/blog/how-to-formulate-research-problem
4. https://www.formpl.us/blog/hypothesis-testing
5. https://www.datapine.com/blog/data-interpretation-methods-benefits-problems/
6. https://leverageedu.com/blog/report-writing/

SCHOOL CORE

Course Code	Course Title	L	T	P	S	C
22EE201002	INNOVATION AND INTELLECTUAL PROPERTY RIGHTS	2	-	-	-	2

Pre-Requisite --

Anti-Requisite --

Co-Requisite --

COURSE DESCRIPTION:

The course is designed to provide comprehensive knowledge to the students regarding the general principles of innovation and intellectual property rights, significance of innovation and steps for innovation, Concept and Theories, Criticisms of Intellectual Property Rights, International Regime Relating to IPR. The course provides an awareness on how to protect ones unique creation, claim ownership, knowledge of what falls under the purview of someone's rights and what doesn't, and safeguard their creations and gain a competitive edge over the peers.

COURSE OUTCOMES: After successful completion of the course, students will be able to:

CO1. Understand the significance of innovation and steps for innovative thinking, and the concepts of intellectual property right and avenues for filling intellectual property rights.

CO2. Understand the legislative practices and protocols for acquisition of trademark and the judicial consequences for violating laws of trademark protection.

CO3. Understand the legislative practices and protocols for acquisition of copyrights and the judicial consequences for violating laws of copyrights protection.

CO4. Understand the fundamentals of patent laws, legislative practices and protocols for acquisition of trade secrets and the judicial consequences for violating laws of trade secrets protection.

CO5. Understand the latest developments and amendments in protection and filling of intellectual rights at international level.

CO-PO Mapping Table:

Course Outcomes	Program Outcomes					
	PO1	PO2	PO3	PO4	PO5	PO6
CO1	-	-	-	-	-	3
CO2	-	-	-	-	-	3
CO3	-	-	-	-	-	3
CO4	-	-	-	-	-	3
CO5	-	-	-	-	-	3
Course Correlation Mapping	-	-	-	-	-	3

Correlation Levels: 3: High; 2: Medium; 1: Low

COURSE CONTENT

Module 1: Introduction to Innovation and IPR (06 Periods)

Innovation: Difference between Creativity and Innovation – Examples of innovation; Being innovative; Identify Blocks for creativity and innovation – overcoming obstacles; Steps for Innovation

Intellectual property rights: Need for intellectual property rights (IPR); types of intellectual property- Design, Geographical Indication; International organizations, agencies and treaties.

Module 2: Trademarks (06 Periods)

Introduction to trademark, Purpose and function of trademarks, acquisition of trade mark rights, protectable matter, selecting and evaluating trade mark, trade mark registration processes.

Module 3: Law of Copyrights (06 Periods)

Fundamental of copy right law, originality of material, rights of reproduction, rights to perform the work publicly, copy right ownership issues, copy right registration, notice of copy right, international copy right law.

Law of patents: Foundation of patent law, patent searching process, ownership rights and transfer.

Module 4: Trade Secrets (06 Periods)

Trade secrete law, determination of trade secrete status, liability for misappropriations of trade secrets, protection for submission, trade secrete litigation.

Unfair competition: Misappropriation right of publicity, false advertising.

Module 5: New Development of Intellectual Property (06 Periods)

New developments in: trade mark law, copy right law, patent law, intellectual property audits. International overview on intellectual property; international - trade mark law, copy right law, international patent law, international development in trade secrets law.

Total Periods: *30*

EXPERIENTIAL LEARNING

1. Should conduct a survey based on the real scenario, where IPR is misused or unethically used and present an article.
2. Prepare an article on the registration processes of IPR practically (copy right/trade mark/ patents).
3. Should study a case of conflict on trademarks/patents and should produce an article mentioning the circumstances and remedial measures.
4. Prepare an article on the latest development in the international intellectual property rights.
5. Refining the project, based on the review report and uploading the text

RESOURCES

TEXT BOOKS:

1. Deborah, E. Bouchoux, *Intellectual property: The law of Trademarks, Copyright, Patents, and Trade Secrets,* Cengage learning, 4th Edition, 2013.
2. Prabuddha Ganguli, *Intellectual property right - Unleashing the knowledge economy*, McGraw Hill Education, 1st Edition, 2017.
3. Tom Kelley & Jonathan Littman, *The Art of Innovation*, Profile Books Ltd, UK, 2008

REFERENCE BOOKS:

1. Neeraj P., & Khusdeep D, *Intellectual Property Rights,* PHI learning Private Limited, 1st Edition, 2019.
2. Nithyananda, K V. *Intellectual Property Rights: Protection and Management*, Cengage Learning India Private Limited, 2019
3. Edward debone, *How to have Creative Ideas*, Vermilon publication, UK, 2007.

VIDEO LECTURES:

1. https://nptel.ac.in/courses/110105139
2. https://www.youtube.com/watch?v=bEusrD8g-dM
3. https://www.youtube.com/watch?v=LS7TTb23nzU

Web Resources:

1. http://www.bdu.ac.in/cells/ipr/docs/ipr-eng-ebook.pdf
2. https://www.wipo.int/edocs/pubdocs/en/intproperty/489/wipo_pub_489.pdf
3. http://cipam.gov.in/
4. https://www.wipo.int/about-ip/en/
5. http://www.ipindia.nic.in/

SCHOOL CORE

Course Code	Course Title	`	T	P	S	C
22EC211001	**INTERNSHIP**	-	-	-	-	2

Pre-Requisite --

Anti-Requisite --

Co-Requisite --

COURSE DESCRIPTION: Expose students to the industrial environment; Create competent professionals for the industry; sharpen the real time skills required at the job; Gain professional experience and understand engineer's technical / managerial responsibilities and ethics; Familiarize with latest equipment, materials and technologies; Gain exposure to technical report writing; Gain exposure to corporate working culture.

COURSE OUTCOMES: After successful completion of this course, the students will be able to:

CO1: Analyze latest equipment, materials and technologies that are used in industry to solve complex engineering problems following relevant standards, codes, policies and regulations.

CO2: Analyze safety, health, societal, environmental, sustainability, economical and managerial factors considered in industry in solving complex engineering problems.

CO3: Perform individually or in a team besides communicating effectively in written, oral and graphical forms on practicing engineering.

CO-PO Mapping Table:

Course Outcomes	Program Outcomes					
	PO1	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**
CO1	3	2	2	2	2	2
CO2	3	2	2	2	2	2
CO3	3	2	2	2	2	2
Course Correlation Mapping	**3**	**2**	**2**	**2**	**2**	**2**

Correlation Level: 3-High; 2-Medium; 1-Low

SCHOOL CORE

Course Code	Course Title	L T P S C
22EC209001	**Project Work Phase-I**	- - - - 10

Pre-Requisite -

Anti-Requisite -

Co-Requisite -

COURSE DESCRIPTION: Identification of topic for the project work; Literature survey; Collection of preliminary data; Identification of implementation tools and methodologies; Performing critical study and analysis of the problem identified; submitting a Report.

COURSE OUTCOMES: After successful completion of the course, students will be able to:

CO1. Apply contextual knowledge to identify specific domain in VLSI and allied areas of discipline.

CO2. Conduct literature review, analyze, cognize and comprehend the extracted information to recognize the current status of research pertinent to the chosen domain.

CO3. Select appropriate tools, techniques and resources for implementation of project work.

CO4. Function effectively as an individual to recognize the opportunities in the chosen domain of interest

CO5. Write and present a technical report/document to present the findings on the chosen problem.

CO6. Engage lifelong learning for development of technical competence in the field of VLSI.

CO-PO Mapping Table:

Course Outcomes	Program Outcomes					
	PO1	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**
CO1	3	2	2	2	2	2
CO2	3	2	2	2	2	2
CO3	3	2	2	2	2	2
CO4	3	2	2	2	2	2
CO5	3	2	2	2	2	2
CO6	3	2	2	2	2	2
Course Correlation Mapping	**3**	**2**	**2**	**2**	**2**	**2**

Correlation Levels: 3: High; 2: Medium; 1: Low

SCHOOL CORE

Course Code	Course Title	L T P S C
22EC210001	**Project Work Phase-II**	- - - - 14

Pre-Requisite -

Anti-Requisite -

Co-Requisite -

COURSE DESCRIPTION: Time and cost analysis; undertaking practical investigations of project work; implementation; analysis of results; validation and report writing.

COURSE OUTCOMES: After successful completion of the course, students will be able to:

CO1. Design and develop Integrated Circuits/systems/platforms to undertake practical investigations of project work, analyze and interpret results.

CO2. Utilize appropriate tools, techniques and resources for implementation of project work.

CO3. Function effectively as an individual to recognize the opportunities in the chosen domain of interest

CO4. Write and present a technical report/document to present the findings on the chosen problem.

CO5. Engage lifelong learning for development of technical competence in the field of VLSI.

CO-PO Mapping Table:

Course Outcomes	Program Outcomes					
	PO1	PO2	PO3	PO4	PO5	PO6
CO1	3	2	2	2	2	2
CO2	3	2	2	2	2	2
CO3	3	2	2	2	2	2
CO4	3	2	2	2	2	2
CO5	3	2	2	2	2	2
Course Correlation Mapping	**3**	**2**	**2**	**2**	**2**	**2**

Correlation Levels: 3: High; 2: Medium; 1: Low

SCHOOL CORE

Course Code	Course Title	L	T	P	S	C
22AI207601	**STATISTICS WITH R**	2	-	-	-	2

Pre-Requisite -

Anti-Requisite -

Co-Requisite -

COURSE DESCRIPTION: This course introduces the basic concepts of statistics using R language. The course also deals with various types of sampling methods and its impact in the scope of inference through the computation of confidence intervals. The topics covered in the course also includes descriptive statistics, marginal and conditional distribution, statistical transformations, chi-squared test and ANOVA.

COURSE OUTCOMES: After successful completion of the course, students will be able to:

CO1. Import, manage, manipulate, structure data files and visualize data using R programming.

CO2. Identify trends and patterns in data using Marginal, Conditional distributions andStatistical transformations.

CO3. Analyse data using sampling and probability distribution methods and compute confidence intervals for statistical inference.

CO4. Apply chi-squared goodness-of-fit test, Pearson's χ 2-statistic and ANOVA to investigatethe distribution of data.

CO-PO Mapping Table:

Course Outcomes	Program Outcomes					
	PO1	PO2	PO3	PO4	PO5	PO6
CO1	3	2	-	-	-	-
CO2	3	2	-	-	-	-
CO3	2	2	-	-	-	-
CO4	3	2	-	-	-	-
Course Correlation Mapping	3	2	-	-	-	-

Correlation Levels: 3: High; 2: Medium; 1: Low

COURSE CONTENT

Module 1: INTRODUCTION ***(05 Periods)***

Data, R's command line, Variables, Functions, The workspace, External packages, Data sets, Data vectors, Functions, Numeric summaries, Categorical data.

Module 2: BIVARIATE AND MULTIVARIATE DATA ***(07 Periods)***

Lists, Data frames, Paired data, Correlation, Trends, Transformations, Bivariate categorical data, Measures of association, Two-way tables, Marginal distributions, Conditional distributions, Graphical summaries, Multivariate data - Data frames, Applying a function overa collection, Using external data, Lattice graphics, Grouping, Statistical transformations.

Module 3 POPULATIONS ***(06 Periods)***

Populations, Discrete random variables, Random values generation, Sampling, Families of distributions, Central limit theorem, Statistical Inference - Significance tests, Estimation, Confidence intervals, Bayesian analysis.

Module 4 CONFIDENCE INTERVALS ***(06 Periods)***

Confidence intervals for a population proportion, p - population mean, other confidence intervals, Confidence intervals for differences, Confidence intervals for the median, Significance test - Significance test for a population proportion, Significance test for the mean (t-tests), Significance tests and confidence intervals, Significance tests for the median.

Module 5 GOODNESS OF FIT ***(06 Periods)***

The chi-squared goodness-of-fit test, The multinomial distribution, Pearson's χ 2-statistic, chi-squared test of independence and homogeneity, Goodness-of-fit tests for continuous distributions, ANOVA - One-way ANOVA, Using *lm* for ANOVA.

Total Periods: 30

EXPERIENTIAL LEARNING

1. The data set baby boom (Using R) contains data on the births of 44 children in a one-day period at a Brisbane, Australia, hospital. Compute the skew of the wt variable, which records birth weight. Is this variable reasonably symmetric or skewed? The variable running.time records the time after midnight of each birth. The command diff(running.time) records the differences or inter-arrival times. Is thisvariable skewed?

2. An elevator can safely hold 3, 500 pounds. A sign in the elevator limits the passenger count to 15. If the adult population has a mean weight of 180 pounds with a 25-pound standard deviation, how unusual would it be, if the central limit theorem applied, thatan elevator holding 15 people would be carrying more than 3, 500 pounds?

3. The data set MLB Attend (Using R) contains attendance data for Major League Baseball between the years 1969 and 2000. Use lm to perform a t-test on attendance for the two levels of league. Is the difference in mean attendance significant? Compare your results to those provided by t-test.

RESOURCES

TEXT BOOKS:

1. John Verzani, *Using R for Introductory Statistics*, CRC Press, 2nd Edition, 2014.
2. Sudha G Purohit, Sharad D Gore, Shailaja R Deshmukh, *Statistics Using R*, Narosa Publishing house, 2nd Edition, 2021.

REFERENCE BOOKS:

1. Francisco Juretig, *R Statistics Cookbook*, Packt Publishing, 1st Edition, 2019.
2. Prabhanjan N. Tattar, Suresh Ramaiah, B. G. Manjunath, *A Course in Statistics with R*, Wiley, 2018.

VIDEO LECTURES:

1. https://onlinecourses.nptel.ac.in/noc21_ma76/preview
2. https://onlinecourses.nptel.ac.in/noc19_ma33/preview
3. https://youtu.be/WbKiJe5OkUU?list=PLFW6lRTa1g83jjpIOte7RuEYCwOJa-6Gz
4. https://youtu.be/svDAkvh6utM?list=PLFW6lRTa1g83jjpIOte7RuEYCwOJa-6Gz
5. https://nptel.ac.in/courses/111104120

WEB RESOURCES:

1. https://www.geeksforgeeks.org/r-statistics/
2. https://www.geeksforgeeks.org/r-programming-exercises-practice-questions-and-solutions/
3. https://www.w3schools.com/r/r_stat_intro.asp
4. https://www.w3schools.com/r/r_stat_intro.asp
5. https://statsandr.com/blog/descriptive-statistics-in-r/

SCHOOL CORE

Course Code	Course Title	L	T	P	S	C
22LG207601	**TECHNICAL REPORT WRITING**	2	-	-	-	2

Pre-Requisite -

Anti-Requisite -

Co-Requisite -

COURSE DESCRIPTION: This course deals withpreparing effective technical documents for both written and digital media, with particular emphasis on technical memos, problem-solving and decision-making reports, and organizational, product-support, and technical-information webs.

COURSE OUTCOMES: After successful completion of the course, students will be able to:

CO1. Demonstrate knowledge of Technical Report Writing and structures with a scientific attitude.
CO2. Analyze the process of writing in preparing effective reports.
CO3. Demonstrate styles of writing for Publication in a Scientific Journal.
CO4. Apply the process of referencing and editing techniques for effective communication in written documents.
CO5. Analyze the strategies in the technical report presentation.

CO-PO Mapping Table:

Course Outcomes	Program Outcomes					
	PO1	PO2	PO3	PO4	PO5	PO6
CO1	-	-	-	-	3	-
CO2	-	-	-	-	3	-
CO3	-	-	-	-	3	-
CO4	-	-	-	-	3	-
CO5	-	-	-	-	3	-
Course Correlation Mapping	**-**	**-**	**-**	**-**	**3**	**-**

Correlation Levels: **3: High;** **2: Medium;** **1: Low**

COURSE CONTENT

Module 1: INTRODUCTION TO TECHNICAL REPORT WRITING ***(06 Periods)***

Concepts of Technical Report, Types of Reports, Planning Technical Report Writing, Components of a Technical Report, Report Writing in Science and Technology, Selecting and Preparing a Title, Language Use in Report Writing.

Module 2: PROCESSOF WRITING ***(06 Periods)***

Writing the 'Introduction', Writing the 'Materials and Methods, Writing the Findings/Results, Writing the 'Discussion', Preparing and using "Tables'.

Module 3: STYLE OF WRITING ***(06 Periods)***

Preparing and using Effective 'Graphs', Citing and Arranging References-I, Citing and Arranging References –II, Writing for Publication in a Scientific Journal.

Module 4: REFERENCING ***(06 Periods)***

Literature citations, Introductory remarks on literature citations, Reasons for literature citations, Bibliographical data according to ISO standards, Citations in the text, Copyright, and copyright laws, the text of the Technical Report, Using a word processing and desktop publishing (DTP) systems, Document or page layout, hints on editing Typographic details, Cross-references.

Module 5: PRESENTATION ***(06 Periods)***

Presentation with appropriate pointing, Dealing with intermediate questions, Review and analysis of the presentation, Rhetoric tips from A to Z.

Total Periods: 30

EXPERIENTIAL LEARNING

1. Prepare a report on technologies of modern times that enriched the originality of research works and their impacts on society concerning plagiarism.
2. Make PowerPoint presentations on the various style of writing academic reports.
3. Error-free Reports are so important for successful communication and sharing of information. Prepare a detailed chart on proofreading techniques to make a report effective and error-free.
4. Design a logo for a company and write down the copy-right laws for that.
5. Read research articles from any international journal of science and technology and differentiate research writing from other academic and non-academic writings.
6. Write an organizational memo Include a heading, introduction, and summary at the beginning of your memo, and present the details of your discussion in a logical order. Use headings and topic or main-idea sentences to clarify the organization.
7. Prepare an appraisal report on the staff performance of your company.
8. Prepare a PowerPoint presentation on the annual performance report of a company.
9. Critically review and write a report on any one of the recently released products.
10. Read the newspaper and write a detailed report about the content coverage and analyse the factors for the popularity of the newspaper.

RESOURCES

TEXTBOOK

1. RC Sharma and Krishna Mohan, "*Business Correspondence and Report Writing",* McGraw-Hill Publishing, 3rd Edition, 2005 (reprint).
2. Patrick Forsyth, "*How to Write Reports and Proposals",* The Sunday Times, Kogan Page, New Delhi, Revised 2nd Edition, 2010.

REFERENCE BOOKS:

1. John Seely, *"The Oxford Writing & Speaking",* Oxford University Press, Indian Edition
2. Anne Eisenberg, "*A Beginner's Guide to Technical Communication"*, McGraw-Hill Education (India) Private Limited, New Delhi, 2013.

VIDEO LECTURES:

1. https://vimeo.com/143714818
2. https://digitalmedia.sheffield.ac.uk/media/002.+The+Anatomy+of+a+Technical+Report/1_u8wntcge

Web Resources:

1. http://www.resumania.com/arcindex.html
2. http://www.aresearchguide.com/writing-a-technical-report.htm
3. http://www.sussex.ac.uk/ei/internal/forstudents/engineeringdesign/studyguides/tec report writing

SCHOOL CORE

Course Code	Course Title	L	T	P	S	C
22MG207601	**PROJECT MANAGEMENT**	2	-	-	-	2

Pre-Requisite -

Anti-Requisite -

Co-Requisite

COURSE DESCRIPTION: To understand the importance of decision-making while implementing any project and interpret and discuss the results of qualitative and quantitative analysis

COURSE OUTCOMES: After successful completion of the course, students will be able to:

CO1 Understand the basic introduction to project management

CO2 Apply the methods of project identification and selection.

CO3 Understand project allocation methods and evaluation.

CO4 Analyse the techniques for project time, review, and cost

CO5 Understand the factors of risk and quality of a project.

CO-PO Mapping Table:

Course Outcomes	Program Outcomes					
	PO1	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**
CO1	2	1	2	1	-	-
CO2	1	1	2	2	-	
CO3	2	2	1	2	1	-
CO4	3	1	2	2	1	-
CO5	2	2	1	2	1	1
Course Correlation Mapping	**2**	**2**	**2**	**2**	**1**	**1**

Correlation Levels: 3: High; 2: Medium; 1: Low

COURSE CONTENT

Module 1: Introduction ***(05 Periods)***

Concept of project management, project definition and key features of projects, project life cycle phases, typical project management issues, basic project activities

Module 2: Project Identification and Selection ***(06 Periods)***

Identification and screening (brainstorming, strength and weakness in the system, environmental opportunities and threats), Project evaluation methods- Payback period, Net present value, Internal rate of return and project evaluation under uncertainty.

Module 3: Project Resource Management ***(07 Periods)***

Scheduling resources, resource allocation methods, project crashing and resource leveling, working of systems, design of systems, project work system design, project execution plan, project procedure manual project control system, planning scheduling and monitoring

Module 4: Time and Cost Management ***(05 Periods)***

Time Management-Network diagram, forward and backward pass, critical path, PERT and CPM, AOA and AON methods, tools for project network, Cost management-earned value method

Module 5: Risk and Quality Management ***(07 Periods)***

Risk identification, types of risk, risk checklist, risk management tactics, risk mitigation and contingency planning, risk register, communication management, Quality assurance and quality control, quality audit, methods of enhancing quality

Total Periods: 30

EXPERIENTIAL LEARNING

1. Refer to any video lecture on project evaluation methods and give a brief seminar using PPT
2. Select any company wherein you will get the details of activities and time and draw the project network diagram and submit a report.
3.

Activity	Predecessor Activity	Normal Time (Weeks)	Crash Time (Weeks)	Normal Cost (Rs.)	Crash Cost (Rs.)
A	-	4	3	8,000	9,000
B	A	5	3	16,000	20,000
C	A	4	3	12,000	13,000
D	B	6	5	34,000	35,000
E	C	6	4	42,000	44,000
F	D	5	4	16,000	16,500
G	E	7	4	66,000	72,000
H	G	4	3	2,000	5,000

Determine a crashing scheme for the above project so that the total project time is reduced by 3 weeks

4. Collect any case study that discusses the process of probability calculation of success of the project and submit a report

RESOURCES

TEXT BOOKS:

1. R.Panneerselvam and P.Senthil Kumar (2013), Project Management, PHI Learning Private Limited.
2. Prasanna Chandra (2014), Projects: Planning, Analysis, Selection, Financing, implementation, and Review.

REFERENCE BOOKS:

1. A Guide to the Project Management Body of Knowledge: (PMBOK Guide) by Project Management Institute, 2013.
2. Gopala Krishnan & Rama Murthy, A Text book of Project Management, McMillan India.
3. S. Choudhary (2004), Project Management, Tata McGraw Hill Publication.

VIDEO LECTURES:

1. https://onlinecourses.nptel.ac.in/noc19_mg30/preview
2. https://archive.nptel.ac.in/courses/110/104/110104073/

Web Resources:

1. https://www.pmi.org/about/learn-about-pmi/what-is-project-management
2. https://www.manage.gov.in/studymaterial/PM.pdf

SCHOOL CORE

Course Code	Course Title	L	T	P	S	C
22MG207602	**ESSENTIALS OF BUSINESS ETIQUETTES**	2	-	-	-	2

Pre-Requisite

Anti-Requisite

Co-Requisite -

COURSE DESCRIPTION: This course is designed for learners who desire to improve their Business etiquette and professionalism.

COURSE OUTCOMES: After successful completion of the course, students will be able to:

CO1. learn the principles of business etiquettes and professional behavior
CO2. understand the etiquettes for making business correspondence effective
CO3. Develop awareness of dining and multicultural etiquettes
CO4. Demonstrate an understanding of professionalism in terms of workplace behaviors and workplace relationships.
CO5. Understand attitudes and behaviors consistent with standard workplace expectations.

CO-PO Mapping Table:

Course Outcomes	Program Outcomes					
	PO1	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**
CO1	1	1	-	-	-	1
CO2	1	1	2	1	-	1
CO3	2	-	2	-	1	-
CO4	1	2	-	1	-	-
CO5	1	2	1	-	-	-
Course Correlation Mapping	**2**	**2**	**2**	**1**	**1**	**1**

Correlation Levels: 3: High; 2: Medium; 1: Low

COURSE CONTENT

Module 1: Business Etiquettes- An Overview ***(06 Periods)***

Significance of Business Etiquettes in 21st Century- Professional Advantage; Need and Importance of Professionalism; Workplace Etiquette: Etiquette for Personal Contact- Personal Appearance, Gestures, Postures, Facial Expressions, Eye-contact, Space distancing

Module 2: Communication Skills ***(06 Periods)***

Understanding Human Communication, Constitutive Processes of Communication, Language as a tool of communication, Barriers to Effective communication, and Strategies to Overcome the Barriers.

Module 3: Teamwork and Leadership Skills ***(06 Periods)***

Concept of Teams; Building effective teams; Concept of Leadership and honing Leadership skills. Personality: Meaning & Definition, Determinants of Personality, Personality Traits, Personality and Organisational Behaviour Motivation: Nature & Importance, Herzberg's Two Factor theory, Maslow's Need Hierarchy theory, Alderfer's ERG theory

Module 4: Interview Skills ***(06 Periods)***

Interview Skills: in-depth perspectives, Interviewer and Interviewee, Before, During and After the Interview, Tips for Success. Meeting Etiquette: Managing a Meeting-Meeting agenda, Minute taking,; Duties of the chairperson and secretary; Effective Meeting Strategies - Preparing for the meeting, Conducting the meeting, Evaluating the meeting

Module 5: Decision-Making and Problem-Solving Skills ***(06 Periods)***

Decision-Making and Problem-Solving Skills: Meaning, Types and Models, Group and Ethical Decision-Making, Problems and Dilemmas in application of these skills. Conflict Management: Conflict - Definition, Nature, Types and Causes; Methods of Conflict Resolution.

Total Periods:30

EXPERIENTIAL LEARNING

LIST OF EXPERIMENTS:

1. Collect the case studies related to successful leaders and their traits.
2. Conduct a mock interview showcasing interview skills.
3. The case studies will be collected as Assignments and the same will be evaluated.

RESOURCES

TEXT BOOKS:

1. Barbara Pachter, Marjorie Brody. Complete Business Etiquette Handbook. Prentice Hall, 2015.
2. Mahanand, Anand. English for Academic and Professional Skills. Delhi: McGraw, 2013. Print.

REFERENCE BOOKS:

1. Pease, Allan and Barbara Pease. The Definitive Book of Body Language. New Delhi: Manjul Publishing House, 2005.
2. Rani, D Sudha, TVS Reddy, D Ravi, and AS Jyotsna. A Workbook on English Grammar and Composition. Delhi: McGraw, 2016.

VIDEO LECTURES:

1. https://www.youtube.com/watch?v=NqlfZOPMqjA
2. http://www.nitttrc.edu.in/nptel/courses/video/109104107/L24.html

Web Resources:

1. http://elibrary.gci.edu.np/bitstream/123456789/685/1/BM-783%20The%20Essential%20Guide%20to%20Business%20Etiquette%20by%20Lillian%20H.%20Chaney%2C%20Jeanette%20S.%20Martin.pdf
2. The Essentials of Business Etiquette: How to Greet, Eat, and Tweet Your Way to Success by Barbara Pachter (Ebook) - Read free for 30 days (everand.com)

PROGRAM CORE

Course Code	Course Title	L	T	P	S	C
22EC202002	**ANALOG CMOS VLSI DESIGN**	3	-	3	-	4.5

Pre-Requisite -

Anti-Requisite -

Co-Requisite -

COURSE DESCRIPTION: This course provides a detailed discussion and hands-on experience on MOS device physics, characteristics of amplifiers, feedback circuits and operational amplifiers, Stability and frequency compensation of operational amplifiers, Nonlinear Analog circuits & other applications.

COURSE OUTCOMES: After successful completion of the course, students will be able to:

CO1. Analyze single stage amplifiers, current mirrors, and differential amplifiers for opamp based data converter applications.

CO2. Analyze the frequency response of various amplifiers along with equivalent noise models, feedback amplifiers and operational amplifiers for improving performance of filters and instrumentation amplifiers.

CO3. Apply appropriate stability and frequency compensation techniques and Bandgap references for stable and high speed designs.

CO4. Apply techniques to develop switched capacitor circuits, oscillators and PLL.

CO-PO Mapping Table:

Course Outcomes	Program Outcomes					
	PO1	PO2	PO3	PO4	PO5	PO6
CO1	3	2	2	-	-	-
CO2	3	2	2	-	-	-
CO3	3	2	3	-	-	-
CO4	3	2	3	-	-	-
Course Correlation Mapping	**3**	**2**	**3**	**-**	**-**	**-**

Correlation Levels: **3: High;** **2: Medium;** **1: Low**

COURSE CONTENT

Module 1: BASIC MOS DEVICE PHYSICS AND SINGLE STAGE AMPLIFIERS ***(11 Periods)***

Basic MOS Device Physics: General Considerations, MOS I/V Characteristics, Second-Order Effects.

Single Stage Amplifiers: Basic Concepts, Common-Source Stage, Source follower, Common Gate Stage, Cascode Stage, Differential Amplifiers-Single Ended and Differential Operation, Basic Differential Pair. Passive and Active Current Mirrors.

Module 2: FREQUENCY RESPONSE AND NOISE CHARACTERISTICS OF AMPLIFIERS ***(08 Periods)***

Frequency Response-General Considerations, Common-Source Stage, Source follower, Common Gate Stage, Cascode Stage, Differential pair.
Noise-Statistical Characteristics of Noise, Noise in Single Stage Amplifiers, Noise in Differential Pairs.

Module 3: FEEDBACK CIRCUITS AND OPERATIONAL AMPLIFIERS ***(10 Periods)***

Feedback Circuits - General considerations, Feedback Topologies, Effect of Loading, Effect of Feedback on Noise.

Operational Amplifiers - General considerations, One-stage Op Amps, Two - stage Op Amps, Gain Boosting, Input range limitations, slew rate, power supply rejection, Noise in Op Amps.

Module 4: STABILITY & FREQUENCY COMPENSATION AND BANDGAP REFERENCES ***(08 Periods)***

Stability & Frequency Compensation: General considerations, Multipole Systems, Phase Margin, Frequency Compensation, Compensation of Two-Stage Op Amps.

Bandgap References: Supply-Independent Biasing, Temperature-independent References, PTAT Current Generation, Constant - Gm Biasing, Speed and Noise Issues.

Module 5: NONLINEAR ANALOG CIRCUITS & APPLICATIONS ***(08 Periods)***

Sampling Switches, Switched-Capacitor Amplifiers, Switched capacitor integrator, Ring oscillators, Simple PLL.

Total Periods: 45

EXPERIENTIAL LEARNING

LIST OF EXERCISES:

1. Model the single stage amplifiers (Common Source Amplifier, Common Drain Amplifier, Common Gate Amplifier) using SPICE Language, develop their schematic and layout to evaluate the Parameters like Gain, Output Resistance, Power Dissipation, etc.
2. Model the Differential Amplifiers using SPICE Language, develop their schematic and layout to evaluate the Parameters like Gain, Output Resistance, Power Dissipation, etc.
3. Model the Cascode Amplifiers using SPICE Language, develop their schematic and layout to evaluate the Parameters like Gain, Output Resistance, Power Dissipation, etc.
4. Model the Operational amplifiers using SPICE Language, develop their schematic and layout to evaluate the Parameters like gain, Output Resistance, Power Dissipation, etc.

5. Model the Feedback Amplifiers using SPICE Language, develop their schematic and layout to evaluate the Parameters like gain, Output Resistance, Power Dissipation, etc.
6. Model and apply the gain boosting techniques to CMOS amplifiers using SPICE Language, develop their schematic and layout to evaluate the Parameters like Gain, Power Dissipation, etc.
7. Model and apply the frequency compensation techniques to CMOS amplifiers using SPICE Language, develop their schematic and layout to obtain their frequency response.
8. Model Bandgap Reference Circuits by using SPICE Language, develop their schematic and layout to obtain their Characteristics.
9. Model Sampling Switches using SPICE Language, develop their schematic and layout to obtain their characteristics.
10. Model Switched Capacitor Amplifier and Integrator using SPICE Language, develop their schematic and layout to obtain their characteristics.
11. Model Ring Oscillator using SPICE Language, develop their schematic and layout to obtain their characteristics.
12. Model Phase Locked Loop using SPICE Language, develop their schematic and layout to obtain their characteristics.

RESOURCES

TEXT BOOKS:

1. Behzad Razavi, *Design of Analog CMOS Integrated Circuit*, Tata-McGrawHill, 2nd Edition 2017.

REFERENCE BOOKS:

1. D.A. John & Ken Martin, *Analog Integrated Circuit Design*, John Wiley, 2nd Edition, 2013.
2. Philip Allen & Douglas Holberg, *CMOS Analog Circuit Design*, Oxford University Press, 3rd Edition, 2013.

SOFTWARE/TOOLS:

1. Software: Cadence/ synopsys/ mentor graphics/ DSCH and Microwind Tools/ Symica TCAD Tools

VIDEO LECTURES:

1. https://nptel.ac.in/courses/117101105
2. https://onlinecourses.nptel.ac.in/noc21_ee51/preview
3. https://www.udemy.com/course/analog_ic_design_overview/

PROGRAM CORE

Course Code	Course Title	L	T	P	S	C
22EC202003	DIGITAL CMOS VLSI DESIGN	3	-	3	-	4.5

Pre-Requisite -

Anti-Requisite -

Co-Requisite -

COURSE DESCRIPTION: This course provides a detailed discussion and hands-on experience on Characteristics of CMOS digital circuits; Transistor sizing; memory design; Design strategies; Design of subsystems.

COURSE OUTCOMES: After successful completion of the course, students will be able to:

CO1. Analyze the characteristics of CMOS Inverter and Design combinational and sequential logic circuits using various design styles.

CO2. Analyze timing issues to improve the performance of sequential logic circuits.

CO3. Design memories and sub systems using CMOS logic for high speed networks.

CO4. Understand design methodologies and tools at various levels of abstraction.

CO-PO Mapping Table:

Course Outcomes	Program Outcomes					
	PO1	PO2	PO3	PO4	PO5	PO6
CO1	3	3	-	-	-	-
CO2	3	3	-	-	-	-
CO3	3	-	-	-	-	-
CO4	3	3	-	-	-	-
Course Correlation Mapping	3	3	-	-	-	-

Correlation Levels: 3: High; 2: Medium; 1: Low

COURSE CONTENT

Module 1: CMOS INVERTER CHARACTERISTICS AND DESIGN STYLES ***(09 Periods)***

MOS Inverters: Introduction, Definitions and Properties, Static CMOS Inverter, Static and Dynamic Power Dissipation, CMOS inverter delay time definitions and calculations.

***Designing Combinational Logic Gates in CMOS*:** Introduction, Static CMOS Design, Dynamic CMOS Design, Domino and NORA logic, Power Consumption in CMOS Gates.

Module 2: DESIGNING SEQUENTIAL LOGIC GATES IN CMOS ***(10 Periods)***

Introduction, Static Sequential Circuits, Dynamic Sequential Circuits, Non-Bistable Sequential Circuit, Logic Style for Pipelined Structures.

Timing Issues in Digital Circuits: Introduction, Clock Skew and Sequential Circuit Performance, Clock Generation and Synchronization

Module 3 HIGH SPEED NETWORK AND MEMORY DESIGN ***(9 Periods)***

Methods of Logical Effort for transistor sizing - Power consumption in CMOS Gates, Low power CMOS design. CMOS Memory design – SRAM, DRAM.

Module 4 SUBSYSTEM DESIGN PROCESS ***(9 Periods)***

General arrangement of 4-bit Arithmetic Processor, Design of 4-bit shifter, Design of ALU sub-system, Implementing ALU functions with an adder, Multipliers, modified Booth's algorithm

Module 5 DESIGN METHODOLOGY AND TOOLS ***(08 Periods)***

Introduction, Structured Design Strategies, Design Methods, Design Flows, Design Economics, Data Sheets and Documentation.

Total Periods: 45

EXPERIENTIAL LEARNING

List of Exercises:

Design, Synthesize and Implement the following logic circuits using LTSpice:

1. CMOS inverter.
2. Transmission Gate.
3. Pseudo static Circuit.
4. True Single phase clocked Edge Triggered Circuit.
5. Bistable Sequential Circuit
6. Astable Sequential Circuit
7. Dynamic CMOS
8. SRAM& DRAM
9. 4-bit shifter
10. ALU sub-system
11. Sequential Circuit with and without Pipelining
12. 4-bit Arithmetic Processor

RESOURCES

TEXT BOOKS:

1. Jan M Rabaey, *Digital Integrated Circuits*, Pearson Education, 2nd Edition, 2003
2. Sung-Mo Kang & Yusuf Leblebici, *CMOS Digital Integrated Circuits,* McGraw Hill, 3rd edition 2003
3. Kamran Eshranghian, Douglas A.Pucknell and Sholeh Eshranghian, *Essential of VLSI Circuits and Systems*, PHI, 1st edition, 2005
4. Neil H. E. Weste, David Money Harris, *CMOS VLSI Design-A Circuit and Systems Perspective*' Pearson, 4th Edition,2011

REFERENCE BOOKS:

1. Eugene D Fabricus, *Introduction to VLSI Design*, McGraw Hill International Edition, 1990
2. John P.Uyemura, *Introduction to VLSI Circuits and Systems*, John Wiley & sons, 1st Edition, 2002

SOFTWARE /TOOLS:

Software: LTSPICE.
Hardware: Personal Computer with necessary peripherals, configuration and operating System.

VIDEO LECTURES:

1. https://www.digimat.in/nptel/courses/video/108107129/L01.html

Web Resources:

1. https://kanchiuniv.ac.in/coursematerials/VLSI%20Design%20_%20GSK.pdf
2. https://www.tutorialspoint.com/vlsi_design/vlsi_design_sequential_mos_logic_circuits.htm
3. https://www.researchgate.net/publication/353463964_Design_and_Optimization_of_4-BIT_Static_RAM_and_4-BIT_Dynamic_RAM_for_Compact_and_Portable_Devices.
4. https://slideplayer.com/slide/5005787/.
5. https://www.researchgate.net/publication/337144112_Enhanced_Modified_Booth_Recoding_Technique_for_Signal_Processing_Application.

PROGRAM CORE

Course Code	Course Title	L	T	P	S	C
22EC202004	VLSI DESIGN VERIFICATION AND TESTING	3	-	3	-	4.5

Pre-Requisite -

Anti-Requisite -

Co-Requisite -

COURSE DESCRIPTION: This course provides knowledge in generation of test vectors for digital systems, to analyse and test various faults in digital system design and develop fault free applications, testing Combinational Circuits and Sequential Circuits, DFT Approaches and BIST Concepts.

COURSE OUTCOMES: After successful completion of the course, students will be able to:

CO1. Analyze Modelling of Digital Circuits at various levels of abstraction and various types of logic Simulations.

CO2. Understand the various fault models, reduction techniques to apply for fault sampling and simulation.

CO3. Apply the automatic test generation techniques for testing Single Stuck at Faults and bridging faults in digital circuits.

CO4. Analyze the various testing approaches and Built-In Self-Test architectures for testing digital circuits.

CO-PO Mapping Table:

Course Outcomes	Program Outcomes					
	PO1	PO2	PO3	PO4	PO5	PO6
CO1	3	-	3	-	-	-
CO2	3	3	-	-	-	-
CO3	3	-	-	-	-	-
CO4	3	-	-	-	-	-
Course Correlation Mapping	3	-	-	-	-	-

Correlation Levels: 3: High; 2: Medium; 1: Low

COURSE CONTENT

Module 1: INTRODUCTION TO TESTING ***(08 Periods)***

Modeling - Modeling Digital Circuits at Logic Level, Register Level and Structural Models. Level of Modeling, Logic Simulation- Types of Simulation, Delay Models, Element Evaluation, Hazard Detection, Gate Level Event Driven Simulation.

Module 2: FAULT MODELING AND SIMULATION ***(9 Periods)***

Logic Fault Models, Fault Detection and Redundancy, Fault Equivalence and Fault Location, Fault Dominance, Fault Simulation Techniques, Fault Sampling.

Module 3 TESTING FOR STUCK FAULTS ***(9 Periods)***

ATG for SSFs in Combinational Circuits and Sequential Circuits, Detection of Non feedback and Feedback Bridging Faults.

Module 4 DESIGN FOR TESTABILITY ***(9 Periods)***

Controllability and Observability, Scan-Based Designs and Architecture, Board-Level and System-Level DFT Approaches, Compression Techniques, Syndrome Testing and Signature Analysis.

Module 5 BUILT-IN SELF TEST ***(10 Periods)***

Introduction to BIST Concepts, Test - Pattern Generation, off-line BIST Architectures, Specific BIST Architectures – CSBL, BEST, RTS, LOCST, STUMPS, CBIST, CEBS, RTD, SST, CATS, CSTP, BILBO.

Total Periods: 45

EXPERIENTIAL LEARNING

List of Exercises:

Generate Lay out, Schematic Design of the following logic circuits using Microwind:

1. CMOS inverter
2. Transmission Gate
3. Basic/ Universal Gates
4. Flip flop -RS, D, JK, MS, T
5. Serial & Parallel adder
6. 4-bit counter [Synchronous and Asynchronous counter]
7. SRAM& DRAM
8. 4-bit shifter
9. ALU sub-system
10. Sequential Circuit with Pipelining
11. Dynamic CMOS
12. 4-bit Arithmetic Processor

RESOURCES

TEXT BOOKS:

1. Miron Abramovici, Melvin A. Breur, Arthur D.Friedman, *Digital Systems Testing and Testable Design*, Wiley, 1st Edition, 1994.

REFERENCE BOOKS:

1. Alfred L. Crouch, *Design for Test for Digital ICs & Embedded Core Systems*, Prentice Hall PTR, 1st Reprint Edition, 1999.
2. Robert J. Feugate, Jr., Steven M.Mclntyre, *Introduction to VLSI Testing*, Prentice Hall, 1st Illustrated Edition, 1998.

SOFTWARE /TOOLS:

Software: Microwind.
Hardware: Personal Computer with necessary peripherals, configuration and operating System.

VIDEO LECTURES:

1. https://www.digimat.in/nptel/courses/video/117103125/L01.html
2. https://nptel.ac.in/courses/117103125
3. https://nptel.ac.in/courses/106103016/21
4. https://nptel.ac.in/courses/106105161/5

Web Resources:

1. http://www2.eng.cam.ac.uk/~dmh/4b7/resource/section16.htm

PROGRAM CORE

Course Code	Course Title	L	T	P	S	C
22EC201005	**DEVICE MODELING**	3	-	-	-	3

Pre-Requisite -

Anti-Requisite -

Co-Requisite -

COURSE DESCRIPTION: This course provides a detailed discussion on MOS Transistor; Small Dimension Effects; Ion Implanted Channels; MOS Transistor in Static and Dynamic operations and its Small signal Modeling.

COURSE OUTCOMES: After successful completion of the course, students will be able to:

CO1. Analyze the multi terminal MOS transistors to improve performance characteristics of digital IC's.

CO2. Analyze Secondary effects of MOSFETs with Ion implanted Channels for VLSI Circuits.

CO3. Develop Quasi static Model and Non Quasi static Models for low, medium and high frequencies.

CO-PO Mapping Table:

Course Outcomes	Program Outcomes					
	PO1	PO2	PO3	PO4	PO5	PO6
CO1	3	-	-	-	-	-
CO2	3	-	-	-	-	-
CO3	3	3	-	-	-	-
Course Correlation Mapping	**3**	**3**	**-**	**-**	**-**	**-**

Correlation Levels: **3: High;** **2: Medium;** **1: Low**

COURSE CONTENT

Module 1: BASIC DEVICE PHYSICS-I: ***(10 Periods)***

Two Terminal MOS Transistor: Flat-band voltage, Potential balance & charge balance, Effect of Gate-substrate voltage on surface condition, Inversion, Small signal capacitance; C-V Characteristics.
Three Terminal MOS Transistor: Contacting the inversion layer, Body effect, Regions of inversion, Pinch-off voltage.

Module 2: BASIC DEVICE PHYSICS-II: ***(12 Periods)***

Four Terminal MOS Transistor: Transistor regions of operation, general charge sheet models, regions of inversion in terms of terminal voltage, strong inversion, weak inversion, moderate inversion, interpolation models, effective mobility, temperature effects, breakdown p-channel MOS FET, enhancement and depletion type, model parameter values, model accuracy.

Module 3 SECONDARY EFFECTS OF MOSFETs ***(10 Periods)***

MOS Transistor with Ion-Implanted Channels: Enhancement nMOS, Depletion nMOS, Enhancement pMOS.
Small dimension effects: Channel length modulation, barrier lowering, two dimensional charge sharing and threshold voltage, punch-through, carrier velocity saturation, hot carrier effects, scaling, effects of surface and drain series resistance, effects due to thin oxides and high doping. Sub threshold regions, Short channel effects.

Module 4 MOS TRANSISTOR IN DYNAMIC OPERATION ***(07 Periods)***

Large Signal modeling: Quasi static operation, Terminal currents in Quasi static operation, Evaluation of Charges in Quasi static operation, Transit time under DC conditions, Limitations of Quasi static Model, Non Quasi static Analysis

Module 5 SMALL SIGNAL MODELING FOR LOW, MEDIUM AND HIGH FREQUENCIES ***(06 Periods)***

low, Medium frequency small signal model for the intrinsic part, Small signal model for Extrinsic Part, A complete Quasi static Model, Y-Parameter models, Non Quasi static Models.

Total Periods: 45

EXPERIENTIAL LEARNING

1. Develop the Complete symmetric strong inversion model with necessary equations.
2. Summarize the effects due to thin oxides and high doping and effects of surface and Drain Series resistance.
3. Model a 3 terminal MOS structure of n+ region for open circuited, short circuited and With biased voltage.

RESOURCES

TEXT BOOKS:

1. Y. Tsividis, *Operations and Modeling of the MOS Transistor,* Oxford university Press, 3rd edition, 2012.

REFERENCE BOOKS:

1. Trond Ytterdal, Yuhua Cheng and Tor Fjeldly, *Device Modeling for Analog and RF CMOS Circuit Design,* Wiley Publication, 2003.
2. Donald A Neamen and Dhrubes Biswas, *Semiconductor Physics and Devices,* Special Indian Edition, 4th edition, 2012.

VIDEO LECTURES:

1. https//archive.nptel.ac.in/courses/117/106/117106033/
2. https://www.digimat.in/nptel/courses/video/117106033/L35.html

PROGRAM CORE

Course Code	Course Title	L	T	P	S	C
22EC201006	**ADVANCED COMPUTER ARCHITECTURE**	3	-	-	-	3

Pre-Requisite -

Anti-Requisite -

Co-Requisite -

COURSE DESCRIPTION:

This course provides a detailed discussion on Parallel computer models and network properties, Principles of scalable performance, Linear and nonlinear pipelining, Multiprocessors and multicomputer, Multi-vector and SIMD computers, Instruction level parallelism, Parallel languages and compilers, Parallel programming tools and environments.

COURSE OUTCOMES: *After successful completion of the course, students will be able to:*

CO1 Apply the knowledge of parallelism and principles of performance to assess the potential and limitations of parallel computing.

CO2 Design linear and nonlinear pipelines with collision free schedules to improve processor performance.

CO3 Analyze various shared memory organizations, cache synchronization and message passing mechanisms for implementing multiprocessor and multi computer systems.

CO4 Investigate the architectures of multiprocessors and SIMD array processors for developing high performance multi-vector computers.

CO5 Use appropriate parallel programming languages, compilers and environments for parallel program development.

CO-PO Mapping Table:

Course Outcomes	Program Outcomes					
	PO1	PO2	PO3	PO4	PO5	PO6
CO1	3	**-**	3	-	-	-
CO2	3	3	-	-	-	-
CO3	3	**-**	-	-	-	-
CO4	3	**-**	-	-	-	-
CO5	3	-	2	-	-	-
Course Correlation Mapping	**3**	**3**	2.5	-	-	-

Correlation Levels: **3: High;** **2: Medium;** **1: Low**

COURSE CONTENT

Module 1: THEORY OF PARALLELISM (10 Periods)

Parallel Computer Models: Elements of modern computers, Evolution of computer architecture, Multiprocessors and multi-computers, Multi¯vector and SIMD computers.

Program and Network Properties: Conditions of parallelism, Program partitioning and scheduling, Program flow mechanisms, Network properties and routing, Static connection networks, Dynamic connection networks – Omega network, Baseline network.

Module 2: PRINCIPLES OF SCALABLE PERFORMANCE AND PIPELINING (08 Periods)

Principles of Scalable Performance: System attributes to performance**,** Performance metrics and measures – Parallelism profile in programs, Mean performance, Efficiency, utilization and quality; Speedup performance laws – Amdahl's law, Gustafson's law.

Pipelining: Linear pipeline processors - Asynchronous and synchronous models, Clocking and timing control, Speedup, efficiency and throughput; Nonlinear pipeline processors - Reservation and latency analysis, Collision-free scheduling, Pipeline schedule optimization.

Module 3: MULTIPROCESSORS AND MULTICOMPUTERS (09 Periods)

Shared Memory Organizations: Interleaved memory organization, Bandwidth and fault tolerance, Memory allocation schemes.

Cache Coherence and Synchronization Mechanisms: The cache coherence problem, Snoopy bus protocols, Directory-based protocols, Hardware synchronization mechanisms.

Module 4: MULTIVECTOR AND SIMD COMPUTERS (08 Periods)

Vector Processing Principles: Vector instruction types, Vector-access memory schemes.

Multi-vector Multiprocessors: Performance-directed design rules, Cray Y-MP, C-90, Fujitsu VP2000, Mainframes and Mini supercomputers.

SIMD Computer Organizations: Implementation models, CM-2 architecture, MasPar MP-1 architecture.

Module 5: INSTRUCTION LEVEL PARALLELISM AND PARALLEL PROGRAM DEVELOPMENT (10 Periods)

Instruction Level Parallelism: Problem definition, Compiler-detected instruction level parallelism, Operand forwarding, Register renaming, Tomasulo's algorithm, Branch prediction, Limitations, Thread level parallelism.

Parallel Program Development: Parallel languages and compilers, Code optimization– Scalar optimization with basic blocks, Local and global optimizations, vectorization and parallelization methods; Software tools and environments for parallel programming.

Total Periods: *45*

Topics for self-study are provided in the lesson plan.

TEXT BOOKS:

1. Kai Hwang, Naresh Jotwani, *Advanced Computer Architecture*, McGraw Hill, 3rd Edition, 2015.

REFERENCE BOOKS:

1. John Hennessy, David Patterson, *Computer Architecture: A Quantitative Approach,* Morgan Kaufmann,6th Edition, 2017.
2. William Stallings, *Computer Organization and Architecture: Designing for Performance*, Pearson Education, 11th Edition, 2018.
3. John Paul Shen, Mikko H. Lipasti, Modern Processor Design: Fundamentals of Superscalar Processors, Waveland Press Inc, 2013.

ADDITIONAL LEARNING RESOURCES:

1. https://nptel.ac.in/courses/106/103/106103206/
2. https://www.coursera.org/learn/comparch
3. https://www.youtube.com/watch?v=K8F8pKYaQcc&list=PL5Q2soXY2Zi-IymxXpH_9vlZCOeA7Yfn9
4. https://www.udemy.com/course/advance-computer-architecture-and-organization/

PROGRAM CORE

Course Code	Course Title	L	T	P	S	C
22EC202007	**EMBEDDED SYSTEMS DESIGN**	3	-	3	-	4.5

Pre-Requisite

Anti-Requisite --

Co-Requisite --

COURSE DESCRIPTION: This course provides a detailed discussion on MSP430 Architecture; Instruction Set; Programming; On-Chip Resources; Communication with peripherals; Embedded system design approaches.

COURSE OUTCOMES: After successful completion of the course, students will be able to:

CO1. Analyse MSP430 Architecture, Instruction Set, addressing modes to develop programs for various control applications using Assembly and Embedded C.

CO2. Solve Problems by analysing MSP430 On Chip Resources such as Timer, Clock System, Low Power Modes/techniques and Interrupt Structure.

CO3. Realize Mixed Signal Processing and Networking Applications, by analysing on-Chip Resources such as Comparator, ADC, Temperature Sensor, PWM and Communication Peripherals.

CO4. Analyse Language, IDE Support, Processor IC & Design Technologies, and System Modelling Techniques to capture behaviour of Embedded Prototype using suitable model.

CO-PO Mapping Table:

Course Outcomes	Program Outcomes					
	PO1	PO2	PO3	PO4	PO5	PO6
CO1	3	-	-	-	-	-
CO2	3	2	2	-	-	-
CO3	3	3	2	-	-	-
CO4	3	2	2			
Course Correlation Mapping	**3**	**3**	**2**	**-**	**-**	**-**

Correlation Levels: 3: High; 2: Medium; 1: Low

COURSE CONTENT

Module 1: ARCHITECTURE OF MSP430 ***(09 Periods)***

Embedded Systems – Introduction, MSP430 - Anatomy of microcontroller, Memory, Software, Pin out (MSP430G2553), Functional Block diagram, Memory, CPU, and Memory mapped input and output, Clock generator; Exceptions- Interrupts and Resets.

Module 2: PROGRAMMING MSP430 ***(09 Periods)***

Development Environment, Aspects of C for Embedded Systems, Assembly Language, Register Organization, Addressing Modes, Constant Generator and Emulated Instructions, Instruction Set, Example programs- Light LEDs, Read input from a switch; Automatic Control-Flashing light by delay, use of subroutines and Functions; Basic Clock System, Interrupts and Low Power Modes.

Module 3 TIMERS AND MIXED SIGNAL SYSTEMS ***(09Periods)***

Timers - Watchdog Timer, RTC, Timer_A, Measurement in capture mode, PWM generation; Mixed Signal Systems- Comparator_A, ADC10 SAADC –Architecture, operation- Single Conversion, Temperature Sensor on ADC10, DTC in ADC10; ADC12 – Comparison with ADC10.

Module 4 COMMUNICATION PERIPHERALS & PROTOCOLS ***(09 Periods)***

MSP430 Communication Interfaces- USART,USCI, USI; Communication Protocols- SPI, Inter-integrated Circuit Bus, USB, CAN

Module 5 EMBEDDED SYSTEM DESIGN **(09 Periods)**

Processor Technology, IC Technology, Design Technology, Tradeoffs. Model *vs* Language, System Modelling – Data Flow Model, FSM, FSMD, HCFSM, PSM, Concurrent Process Model & implementation.

Total Periods: 45

EXPERIENTIAL LEARNING

I. Introduction to MSP430 launch pad and Programming Environment.

II.
1. Practice on usage of Instruction Set
2. Read input from switch and Automatic control/flash LED (software delay).
3. Interrupts programming example using GPIO.
4. Configure watchdog timer in watchdog & interval mode.
5. Configure timer block for signal generation (with given frequency).
6. Read Temperature of MSP430 with the help of ADC.
7. Test various Power Down modes in MSP430.
8. Generation of Pulse Width Modulation.
9. Use Comparator to compare the signal threshold level.
10. Speed Control of DC Motor
11. Master slave communication between MSPs using SPI.
12. Networking MSPs using Wi-Fi System modelling using FSM.
13. UML as design tool.
14. Networks for embedded systems – SPI, I2C in proteus.
15. Sensors using SPI, State Machines for I2C Communication.

RESOURCES

TEXT BOOKS:

1. John H. Davies, *MSP430 Microcontroller Basics*, Newnes Publications, 1st Edition, 2008
2. Santanu Chattopadyay, *Embedded System Design*, PHI, 2010.
3. Frank Vahid, Tony D. Givargis, *Embedded System Design – A Unified Hardware/Softwar Introduction*, John Wiley, 2006

REFERENCE BOOKS:

1. Chris Nagy, *Embedded Systems Design using the TI MSP30 Series*, Newnes Publications 2003.
2. JorgeonStaunstrup, Wayne Wolf, *Hardware/Software Co-design Principles and Practice* Springer 2009.
3. Patrick R Schamont, *A Practical Introduction to Hardware/Software Co-design*, Springe publications, 2010
4. Raj Kamal, *Embedded systems Architecture, Programming and Design*, Tata McGraw- Hil 2016.

SOFTWARE /TOOLS:

1. Software: Code Composer Studio, Energia, Proteus
2. Hardware: MSP430 launch pad, Wi-Fi booster pack, Associated accessories

VIDEO LECTURES:

1. https://nptel.ac.in/courses/108102045

Web Resources:

1. https://www.udemy.com/course/embedded-system-design-using-uml-state-machines/

PROGRAM ELECTIVE

Course Code	Course Title	L	T	P	S	C
22EC201008	**NETWORK-ON-CHIP DESIGN**	3	-	-	-	3

Pre-Requisite - Co Design, System-on-Chip Design

Anti-Requisite -

Co-Requisite -

COURSE DESCRIPTION: This course provides a detailed discussion on NOC –Architecture Design, Switching Technique; Routing Algorithm ;Fault tolerance; Testing;3D NOC ;Optical NOC.

COURSE OUTCOMES: After successful completion of the course, students will be able to:

CO1 Understand Network on-chip topologies, routing strategies and architectures to improve Quality of Service in communication applications.

CO2 Develop routing algorithms to solve problems of congestion and flow in multicast routing for 2D and 3D Mesh Networks.

CO3 Apply Security and Monitoring Services to reduce the occurrence of dead and Live lock condition during data transmission and Fault tolerance.

CO4 Analyze three-Dimensional Integration of Network-On-Chip for the development of Optical and 3D Network-On-Chip Architectures.

CO-PO Mapping Table:

Course Outcomes	Program Outcomes					
	PO1	PO2	PO3	PO4	PO5	PO6
CO1	3	-	-	-	-	-
CO2	3	-	-	-	-	-
CO3	3	3	-	-	-	-
CO4	3	3	2	-	-	-
Course Correlation Mapping	**3**	**3**	**2**	**-**	**-**	**-**

Correlation Levels: 3: High; 2: Medium; 1: Low

COURSE CONTENT

Module 1: INTRODUCTION TO NOC (09 Periods)

Introduction to NoC, OSI layer rules in NoC, Interconnection Networks in Network-on-Chip Network Topologies, Switching Techniques, Routing Strategies, Flow Control Protocol Quality-of-Service Support-Optical NOC.

Module 2: ARCHITECTURE DESIGN (09 Periods)

Switching Techniques and Packet Format, Asynchronous FIFO Design, GALS Style of Communication, Wormhole Router Architecture Design, VC Router Architecture Design, Adaptive Router Architecture Design.

Module 3: ROUTING ALGORITHM (08 Periods)

Packet routing-QoS, congestion control and flow control, router design, network link design, Efficient and Deadlock-Free Tree-Based Multicast Routing Methods, Path-Based Multicast Routing for 2D and 3D Mesh Networks, Fault-Tolerant Routing Algorithms, Reliable and Adaptive Routing Algorithms.

Module 4: TEST AND FAULT TOLERANCE OF NOC (10 Periods)

Formal Verification of Communications in Networks, on-Chips Test and Fault Tolerance for Networks-on-Chip Infrastructures, Monitoring Services for Networks-on Chips.

Module 5: THREE-DIMENSIONAL INTEGRATION OF NETWORK-ON-CHIP: (09 Periods)

Three-Dimensional Networks-on-Chips Architectures, A Novel Dimensionally-Decomposed Router for On-Chip Communication in 3D Architectures, Resource Allocation for QoS On-Chip Communication,

Total Periods: *45*

Topics for self-study are provided in the lesson plan.

EXPERIENTIAL LEARNING

1. Develop a Network-On-Chip Architecture with Synchronous and Asynchronous FIFO design.
2. Design a 8 port Network-On-Chip router with appropriate analysing technique
3. Examine the fault tolerance techniques of Network-On-Chip Infrastructure.
4. Illustrate 3D Architectural view of Network-On-Chip Architecture.

RESOURCES

TEXT BOOKS:

1. Chrysostomos Nicopoulos, Vijay krishnan Narayanan, Chita R.Das, "*Networks-on – Chip Architectures Holistic Design Exploration*", Springer.1st Edition, 2010.

REFERENCE BOOKS:

1. Fayezge bali, Haythamelmiligi, Hqhahed Watheq E1-Kharashi "Networks-on-Chips theory and practice", 1ST Edition,2017CRC press.
2. Konstantinos Tatas and Kostas Siozios "Designing 2D and 3D Network-on-Chip Architectures" 1ST Edition,2014.
3. Palesi, Maurizio, Daneshtalab, Masoud "Routing Algorithms in Networks-on-Chip" 1ST Edition ,2014.
4. Santanu Kundu, Santanu Chattopadhyay "Network-on-Chip: The Next Generation of System on-Chip Integration", 1ST Edition,2017 CRC Press.

Web Resources:

1. Network on Chip – an Overview | ignitarium.com
2. Multi-Core Computer Architecture – Storage and Interconnects - Course (nptel.ac.in)
3. Networks on Chips: Structure and Design Methodologies (hindawi.com)
4. Microsoft PowerPoint - Ginosar NOC Tutorial ESA Sept 2009 for PDF.ppt

PROGRAM ELECTIVE

Course Code	Course Title	L	T	P	S	C
22EC201009	**IC FABRICATION**	3	-	-	-	3

Pre-Requisite -

Anti-Requisite -

Co-Requisite -

COURSE DESCRIPTION: This course provides a detailed discussion on Crystal Growth, Wafer Preparation, Epitaxy and Oxidation, Lithography and Reactive Plasma Etching, Deposition, Diffusion, Ion Implantation, Metallization, Analytical, Assembly and Packaging Techniques.

COURSE OUTCOMES: After successful completion of the course, students will be able to:

CO1. Analyze Wafer preparation methods, oxidation Techniques, Lithography methods, Etching process, Deposition, Diffusion and Ion-Implantation methods for integrated circuit(IC) fabrication.

CO2. Select and apply appropriate oxidation Techniques, Lithography methods, Etching process, Deposition, Diffusion and Ion-Implantation methods for integrated circuit(IC) fabrication.

CO3. Apply appropriate, metallization films, packaging techniques in IC fabrication.

CO-PO Mapping Table:

Course Outcomes	Program Outcomes					
	PO1	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**
CO1	3	-	-	-	-	-
CO2	3	2	1	-	-	-
CO3	3	3	1	-	-	-
Course Correlation Mapping	**3**	**3**	**1**	-	-	-

Correlation Levels: **3: High;** **2: Medium;** **1: Low**

COURSE CONTENT

Module 1: Crystal Growth (09 Periods)

Introduction to Semiconductor Manufacturing and fabrication, Clean Room types and Standards, Electronic grade silicon, Czochralski crystal growing, silicon shaping.

Module 2: Epitaxy and Oxidation (09 Periods)

Epitaxy: Vapor-phase epitaxy, Molecular beam epitaxy, Epitaxial Evaluation.
Oxidation: Growth mechanism and kinetics; Oxidation Techniques and systems, Oxide properties, Oxidation of polysilicon, Oxidation-Induced defects.

Module 3: Lithography and Etching (09 Periods)

Lithography: Optical lithography, Electron lithography, X-ray lithography
Etching: Feature size control and Anisotropic Etch mechanisms, Properties of Etch Processes, Reactive plasma etching Techniques and Equipments.

Module 4: Deposition, Diffusion and Ion Implantation (09 Periods)

Deposition: Deposition process, Plasma Assisted deposition
Diffusion: The Diffusion Process , Mathematical Model for Diffusion, The Diffusion coefficient , Successive Diffusions, Diffusion Systems,
Ion Implantation: Implantation Technology, Mathematical Model for Ion Implantation, Selective Implantation, Channeling, Lattice Damage and Annealing, Shallow Implantations.

Module 5: Metallization and packaging (09 Periods)

Metallization applications, Metallization choices, Physical Vapor Deposition, Metal Interconnections and Contact Technology, Silicides and Multilayer-Contact Technology, Copper Interconnects and Damascene Processes, Wafer Thinning and Die Separation, Die Attachment, Wire Bonding, Packages, Yield.

Total Periods: *45*

EXPERIENTIAL LEARNING

1. Model the fabrication process flow of NMOS using TCAD tool
2. Model the fabrication process flow of PMOS using TCAD tool
3. Model the fabrication process flow of CMOS using TCAD tool
4. Model the fabrication process flow of PN junction diode using TCAD tool
5. Model the fabrication process flow of BJT junction diode using TCAD tool

RESOURCES

TEXT BOOKS:

1. S.M. Sze, *VLSI technology*, Tata McGraw-Hill, Second Edition, 2017.
2. R.C. Jaeger, *Introduction to microelectronic fabrication*, Prentice Hall, Second Edition, 2013.

REFERENCE BOOKS:

1. Simon M. Sze, Gary S. May, *Fundamentals of Semiconductor Fabrication*, Wiley, 2011

VIDEO LECTURES:

1. https://nptel.ac.in/courses/117106093

WEB RESOURCES:

1. https://1lib.in/book/2379383/784b53

PROGRAM ELECTIVE

Course Code	Course Title	L	T	P	S	C
22EC202010	**NANO MATERIALS AND NANOTECHNOLOGY**	3	-	3	-	4.5

Pre-Requisite IC Fabrication

Anti-Requisite -

Co-Requisite -

COURSE DESCRIPTION:

This course provides a detailed discussion and hands-on experience on Nanostructures – Classification and Peculiarities, Characterization and Properties of Nanomaterials, Micro Electro-Mechanical Systems (MEMS) & Nano Electro-Mechanical Systems (NEMS), Carbon Nanotubes (CNT) – Properties and Synthesis, Interdisciplinary Applications of Nanomaterials.

COURSE OUTCOMES: After successful completion of the course, students will be able to:

CO1 Understand the peculiarities of Nanostructured materials, their characterization and properties to solve structural, mechanical and electrical problems in manufacturing Nanostructures.

CO2 Use IC Fabrication techniques to manufacture Micro Electro-Mechanical Systems (MEMS) and Nano Electro-Mechanical Systems (NEMS).

CO3 Understand carbon nanotube properties and its synthesis for various applications.

CO4 Apply the properties of nanomaterials by fixing the boundaries in system development in multidisciplinary areas like Automobiles, Biomedical, and Agriculture.

CO-PO Mapping Table:

Course Outcomes	Program Outcomes					
	PO1	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**
CO1	3	-	-	-	-	-
CO2	3	2	3	-	-	-
CO3	3	3	-	-	-	-
CO4	3	2	-	-	-	-
Course Correlation Mapping	**3**	**1**	**1**	-	-	-

Correlation Levels: 3: High; 2: Medium; 1: Low

COURSE CONTENT

Module 1: Nanostructures and Peculiarities of Nanostructured Materials (09 Periods)

Gleiter's classification of nanostructured materials, Classification of nanostructures by dimensionality, Concept of "surface form engineering" in nanomaterial science, Extended internal surface, Increasing of surface energy and tension, Grain boundaries, Instability of 3D0 NSM due to grain growth.

Module 2: Characterization and Properties of Nanomaterials (09 Periods)

Structural Characterization: X-ray diffraction (XRD),Scanning electron microscopy (SEM), Transmission electron microscopy (TEM), Chemical Characterization: Optical spectroscopy, Electron spectroscopy, Ionic spectrometry, Physical Properties of Nanomaterials: Melting points and lattice constants, Mechanical properties, Optical properties Electrical conductivity.

Module 3: Micro Electro-Mechanical Systems (MEMS) and Nano Electro-Mechanical Systems (NEMS) (09 Periods)

Introduction, Fabrication of MEMS and NEMS, Surface micromachining, Bulk Micromachining, Fabrication stages, Deposition, Patterning, Etching.

Module 4: Carbon Nanotubes (CNT) (09 Periods)

CARBON NANOTUBES AND RELATED STRUCTURES: PRODUCTION AND FORMATION Introduction-Carbon Nanotube Production-Catalysts-Growth Enhancement-Growth Mechanisms Functionalization-Purification
LAYER-BY-LAYER ASSEMBLY OF MULTIFUNCTIONAL CARBON NANOTUBE THIN FILMS Introduction-Structure and Properties of CNTs-Structural Organization in Multilayers of Carbon Nanotubes-Electrical Conductor Applications-Sensor Applications-Fuel Cell Applications Nano-/Microshell LBL Coatings and Biomedical Applications

Module 5: Interdisciplinary Arena of Nanomaterials (09 Periods)

Molecular Electronics and Nanoelectronics, Nanobots, Biological Applications of Nanoparticles, Catalysis by Gold Nanoparticles, Band Gap Engineered Quantum Devices, Nanomechanics Carbon Nanotube Emitters, Photo electrochemical Cells, Photonic Crystals and Plasmon Waveguides.

Total Periods: *45*

EXPERIENTIAL LEARNING

LIST OF EXERCISES:

1. Compute the Resistance of a Wire using COMSOL 3D Model
2. Compute the Inductance of a Wire using COMSOL 3D Model
3. Compute the Effect of Fringing Fields on Capacitance using COMSOL 3D Model
4. Compute a ZnO nano rods based piezo electric device using COMSOL 3D Model
5. Construct 3D model of MOSFET using COMSOL and verify its results analytically
6. Model a solenoid with spring return using MATLAB
7. Model a semiconductor photovoltaic cell using MATLAB
8. Develop a model using COMSOL and find the Impedance of a Coaxial Cable
9. Design a model of microstrip patch antenna using COMSOL and verify using MATLAB
10. Design and optimize the thickness of thin film deposition in COMSOL

RESOURCES

TEXT BOOKS:

1. A I Gusev and A ARempel, *Nanocrystalline Materials*, Cambridge International Science Publishing, 1st Indian edition, 2008.
2. Guozhong Cao and Ying Wang, *Nanostructures and Nanomaterials: Synthesis, Properties, and Applications,* Imperial College Press, 2004.

REFERENCE BOOKS:

1. Bhushan, Bharat, *Springer Handbook of Nanotechnology*, 2nd edition, 2006.
2. Pokropivny, Vladimir, RynnoLohmus, Irina Hussainova, Alex Pokropivny, and Sergey Vlassov, *Introduction to nanomaterials and nanotechnology*, Tartu, Estonia: Tartu University Press, 2007
3. *Dirk M. Guldi, Nazario Martín, Carbon Nanotubes and Related Structures: Synthesis, Characterization, Functionalization, and Applications,* Wiley-VCH, March 2010

VIDEO LECTURES:

1. https://nptel.ac.in/courses/118104008
2. https://nptel.ac.in/courses/118102003
3. https://onlinecourses.nptel.ac.in/noc21_mm38/

PROGRAM ELECTIVE

Course Code	Course Title	L	T	P	S	C
22EC202011	**LOW POWER CMOS VLSI DESIGN**	3	-	3	-	4.5

Pre-Requisite - Digital CMOS VLSI Design

Anti-Requisite -

Co-Requisite -

COURSE DESCRIPTION: This course provides a detailed discussion and hands-on experience on low power VLSI chips, Sources of Power dissipation in MOS & CMOS Devices, Power Estimation, Synthesis of low power VLSI Circuits, Design of low power VLSI Circuits, Low power Memory Architectures, Energy recovery Circuits, Software design of low power VLSI Circuits.

COURSE OUTCOMES: After successful completion of the course, students will be able to:

CO1. Analyze the various power dissipation effects and estimation methods in CMOS VLSI Circuits to improve the performance characteristics of digital systems.

CO2. Understand the various design styles and synthesis of low power and low voltage CMOS VLSI circuits.

CO3. Analyze the various low power Static RAM architectures in design and development of Ultra Low power Integrated Circuits.

CO4. Apply energy recovery techniques to evaluate the performance of low power VLSI Circuits for scientific research in design and development of digital systems.

CO-PO Mapping Table:

Course Outcomes	Program Outcomes					
	PO1	PO2	PO3	PO4	PO5	PO6
CO1	3	-	-	-	-	-
CO2	3	-	-	-	-	-
CO3	3	-	3	-	-	-
CO4	3	-	3	-	-	-
Course Correlation Mapping	**3**	**-**	**3**	**-**	**-**	**-**

Correlation Levels: 3: High; 2: Medium; 1: Low

COURSE CONTENT

Module 1: POWER DISSIPATION IN CMOS VLSI DESIGN (09 Periods)

Need for low power VLSI chips, Sources of Power dissipation, Power dissipation in MOS & CMOS Devices, Limitations of low Power design.

Module 2: POWER ESTIMATION (09 Periods)

Modelling of Signals, Signal Probability Calculation, Probabilistic Techniques for Signal activity Estimation, Statistical Techniques, Estimation of Glitching Power, Sensitivity Analysis, Power Estimation using input vector Compaction, Estimation of Maximum Power.

Module 3: SYNTHESIZE AND TEST FOR LOW POWER CMOS CIRCUITS (08 Periods)

Synthesis for Low Power: Behavioural Level Transforms, Logic Level optimization of low power, Circuit level.
Design and Test of Low Voltage CMOS Circuits: Circuit Design Style, Leakage current in Deep Sub micrometer Transistors, Low voltage Circuit Design Techniques, Multiple Supply Voltages.

Module 4: LOW POWER STATIC RAM ARCHITECTURES: (10 Periods)

Organization of Static RAM, MOS Static RAM Memory Cell, Banked Organization of SRAMs, Reducing Voltage Swing in Bit lines, Reducing Power in Sense Amplifier Circuits.

Module 5: ENERGY RECOVERY TECHNIQUES AND SOFTWARE DESIGN: (09 Periods)

Low Energy Computing using Energy Recovery Techniques: Energy Recovery Circuit Design, Designs with partially Reversible logic, Supply Clock Generation.
Software design for low power: Sources of software power dissipation, software power estimation, Software power estimation, Co-design for low power.

Total Periods: *45*

Topics for self-study are provided in the lesson plan.

EXPERIENTIAL LEARNING

1. Develop4MB and 16MB SRAM, advanced SRAM Architectures.
2. Design and Explain working principle of Energy recovering technique.
3. Examine the testing technique used in circuit design style and leakage current in deep submicrometric transistors.
4. Illustrate high density packaging methodology on 3Dmemory stacks and MCMs.
5. Estimate glitching power and Signal Probability Calculation in probabilistic techniques.

RESOURCES

TEXT BOOKS:

1. Kaushik Roy, Sharat Prasad, *"Low-Power CMOS VLSI Circuit Design"* Wiley Studen Edition,2000.
2. Gary Yeap, Practical Low-Power Digital VLSI Design, Springer Publication, 1998.

REFERENCE BOOKS:

1. Kiat-Seng Yeo, Samir S.Rofail and Wang-Ling Goh, "*CMOS/BiCMOS ULSI: Low power, Lo Voltage* ",Pearson education,2002.

Web Resources:

1. https://www.hindawi.com/journals/jece/2012/509465/
2. https://nptel.ac.in/courses/106103183/22
3. https://www.electronics-notes.com/articles/electronic_components/semiconductor-ic-memory/memory-types-technologies.php

PROGRAM ELECTIVE

Course Code	Course Title	L	T	P	S	C
22EC201012	**CMOS RF CIRCUIT DESIGN**	3	-	-	-	3

Pre-Requisite - Analog CMOS VLSI Design

Anti-Requisite -

Co-Requisite -

COURSE DESCRIPTION: This course provides a detailed discussion on Basic Concepts of RF Circuits, Transceiver Architectures, Low Noise Amplifier, Mixers, Oscillators, Phased Locked Loops and Power Amplifiers.

COURSE OUTCOMES: After successful completion of the course, students will be able to:

CO5. Apply RF concepts to solve problems in Transceiver Architectures.

CO6. Design LNA using various topologies and RF Mixers.

CO7. Apply the concepts of Feedback to develop different RF Oscillators.

CO8. Design different types of PLLs and Analyse various Large Signal RF Circuits.

CO-PO Mapping Table:

Course Outcomes	Program Outcomes					
	PO1	PO2	PO3	PO4	PO5	PO6
CO1	3	2	3	-	-	-
CO2	3	3	3	-	-	-
CO3	3	2	3	-	-	-
CO4	3	3	3	-	-	-
Course Correlation Mapping	**3**	**3**	**3**	**-**	**-**	**-**

Correlation Levels: 3: High; 2: Medium; 1: Low

COURSE CONTENT

Module 1: BASIC CONCEPTS IN RF DESIGN ***(09 Periods)***

Introduction to RF Design, Time Variance and Nonlinearity, Effects of nonlinearity, random processes and Noise, Definitions of sensitivity and dynamic range, Passive impedance transformation, Scattering parameters.

Module 2: TRANSCEIVER ARCHITECTURES ***(09 Periods)***

General considerations, Receiver Architectures - Modern heterodyne receivers, Direct conversion receivers, Image-Reject receivers. Transmitter Architectures - Modern direct conversion Transmitters, Heterodyne Transmitters.

Module 3: LNA AND MIXERS ***(08 Periods)***

LNA - General considerations, Problem of input matching, LNA Topologies, Gain Switching, Band Switching.

Mixers - General considerations, Passive down conversion mixers, Active down conversion mixers, Up conversion mixers.

Module 4: OSCILLATORS ***(09 Periods)***

Performance parameters, Basic principles, Cross coupled oscillator, Three point oscillators, Voltage Controlled Oscillators, Phase Noise, Mathematical model of VCOs, Quadrature Oscillators.

Module 5: PLL AND POWER AMPLIFIER ***(10 Periods)***

PLLs - Phase Detector, Type-I PLLs, Type-II PLLs, PFD/CP Non-idealities, Phase noise in PLLs, Loop Bandwidth.

Power Amplifiers - General considerations, Classification of power amplifiers, High- Efficiency power amplifiers, Cascode output stages, Large signal impedance matching, Linearization techniques.

Total Periods: 45

EXPERIENTIAL LEARNING

1. Develop a Transceiver circuit and extract the related parameters using VLSI based CAD Tool.
2. Simulate layout in a VLSI based CAD Tool.
3. Optimize the layout for various goals like area, delay and power.

RESOURCES

TEXT BOOKS:

1. B. Razavi, "RF Microelectronics", Pearson Education India, 2nd Edition, 2013.

REFERENCE BOOKS:

1. T. H. Lee, "The Design of CMOS Radio-Frequency Integrated Circuits", Cambridge University Press, 2nd, 2004.
2. R. Jacob Baker, "CMOS Circuit Design, Layout and Simulation", Wiley, 1st Edition, 2009.

VIDEO LECTURES:

1. https://nptel.ac.in/courses/117102012

Web Resources:

1. https://www.ee.iitm.ac.in/~ani/2011/ee6240/lectures.html
2. https://freebookcentre.net/electronics-ebooks-download/RF-Integrated-Circuits-Note-by-NPTEL.html

PROGRAM ELECTIVE

Course Code	Course Title	L	T	P	S	C
22EC201013	**SYSTEM-ON-CHIP DESIGN**	3	-	-	-	3

Pre-Requisite Digital CMOS VLSI Design

Anti-Requisite -

Co-Requisite -

COURSE DESCRIPTION: This course provides a detailed discussion on System on Chip Design Process; System level Design Issues; Test Strategies; Macro Design and Verification; Reusable Macros; System on Chip Verification; Communication Architectures for SoCs.

COURSE OUTCOMES: After successful completion of the course, students will be able to:

CO1. Understand various SoC Design aspects and issues in low power and high speed Implementations.

CO2. Analyze the Macro Design Process to solve issues in usage of hard macros and Develop reusable macros for system integration.

CO3. Analyze verification methods at system level, block level and Hardware/Software Co-verification to reduce the test time.

CO4. Apply various communication architectures to design energy efficient systems.

CO-PO Mapping Table:

course Outcomes	Program Outcomes					
	PO1	PO2	PO3	PO4	PO5	PO6
CO1	3	**-**	-	-	-	-
CO2	3	1	-	-	-	-
CO3	3	2	3	-	-	-
CO4	3	2	3	-	-	-
Course Correlation Mapping	**3**	**1**	**3**	**-**	**-**	**-**

Correlation Levels: 3: High; 2: Medium; 1: Low

COURSE CONTENT

Module 1: SYSTEM ON CHIP DESIGN PROCESS ***(08 Periods)***

A canonical SoC Design, SoC Design flow- waterfall vs spiral, top down vs Bottom up. Specification requirement, Types of Specification, System Design process, System level design issues - Soft IP Vs Hard IP, Design for timing closure - Logic design issues, Verification strategy, Onchip buses and interfaces, Design for Low Power, Manufacturing test strategies.

Module 2: MACRO DESIGN PROCESS ***(07 Periods)***

Overview of IP Design, planning and Specification, Macro Design and Verification, Soft Macro Productization, Developing hard macros - Design issues for hard macros, Model Development for Hard Macros. System Integration with reusable Macros.

Module 3 SOC VERIFICATION - I ***(12 Periods)***

Technology Challenges, Verification technology options, Verification methodology, Test bench Creation, Test bench Migration, Verification languages, Verification IP Reuse, Verification approaches, Verification and Device Test, Verification plans, Bluetooth SoC. System level verification – System Design, System Verification. Block level verification – IP Blocks, Block Details of Bluetooth SoC, Lint Checking, Formal Model Checking, Functional Verification/Simulation, Protocol Checking, Directed Random Testing, Code Coverage Analysis.

Module 4 SOC VERIFICATION - II ***(12 Periods)***

Hardware/Software Co-verification- HW/SW Co-verification Environment, Emulation, soft or virtual Prototypes, Co-verification, UART Co-verification, Rapid Prototype Systems, Software Testing. Static netlist verification, Physical Verification and Design Signoff, Introduction to VMM (Verification Methodology Manual), OVM(Open Verification Methodology) and UVM (Universal Verification Methodology).

Module 5 DESIGN OF COMMUNICATION ARCHITECTURES FOR SOCS ***(06 Periods)***

On chip communication architectures, System level analysis for designing communication, Design space exploration, Adaptive communication architectures-Communication architecture tuners. Communication architectures for energy/battery efficient systems. Introduction to bus functional models and bus functional model based verification**.**

Total Periods: 45

EXPERIENTIAL LEARNING

1. Model Bluetooth transceiver using HDL in VLSI CAD Tools.
2. Model Bluetooth SoC IP using HDL in VLSI CAD Tools.
3. Model UVM architecture for testing real time SoCs.

RESOURCES

TEXT BOOKS:

1. Michael Keating, Pierre Bricaud, *Reuse Methodology manual for System On A Chip Designs*, Kluwer Academic Publishers, 3rdEdition, 2002.
2. Prakash Rashinkar, Peter Paterson and Leena Singh, *SoC Verification Methodology and Techniques*, Kluwer Academic Publishers, 2002.
3. A.A. Jerraya, W.Wolf, *Multiprocessor Systems-on-chips*, M K Publishers, 2005.

REFERENCE BOOKS:

1. William K. Lam, *Hardware Design Verification: Simulation and Formal Method based Approaches*, Prentice Hall, 1st Edition, 2005.
2. Farzed Nekoogar, Faranak Nekoogar, *From ASICs to SOCs: A Practical Approach*, Prentice Hall PTR, 2003.

VIDEO LECTURES:

1. https://nptel.ac.in/courses/108102045/10
2. https://nptel.ac.in/courses/106102181/2
3. https://nptel.ac.in/courses/108102045/

Web Resources:

1. https://www.ee.ryerson.ca/~courses/coe838/lectures/Intro-SoC.pdf
2. https://slideplayer.com/slide/8148235/
3. https://www.cerc.utexas.edu/~jaa/soc/lectures/14-2.pdf
4. https://www.cs.ccu.edu.tw/~pahsiung/courses/soc/notes/04_Verify.pdf

PROGRAM ELECTIVE

Course Code	Course Title	L	T	P	S	C
22EC202014	**MIXED SIGNAL DESIGN**	3	-	3	-	4.5

Pre-Requisite Analog CMOS VLSI Design

Anti-Requisite -

Co-Requisite -

COURSE DESCRIPTION: This course provides a detailed discussion and hands-on experience on Switched capacitor circuits - analysis and application, Design and characterization of Phase locked loops, Data converters – types, Design for different sampling rates.

COURSE OUTCOMES: After successful completion of the course, students will be able to:

CO1. Analyze switched capacitor circuits, integrators, filters and phase locked loops to improve performance characteristics for multidisciplinary applications.

CO2. Analyze the process of data conversion as applicable to data converters.

CO3. Analyze various methodologies and limitations in designing analog to digital converters with nyquist rate.

CO4. Apply the concepts of oversampling and develop mixed signal circuits like high speed modulators, interpolating & decimating filters for multidisciplinary applications.

CO-PO Mapping Table:

Course Outcomes	Program Outcomes					
	PO1	PO2	PO3	PO4	PO5	PO6
CO1	3	-	-	-	-	-
CO2	3	-	-	-	-	-
CO3	3	2	3	-	-	-
CO4	3	2	3	-	-	-
Course Correlation Mapping	**3**	**2**	**3**	**-**	**-**	**-**

Correlation Levels: 3: High; 2: Medium; 1: Low

COURSE CONTENT

Module 1: SWITCHED CAPACITOR CIRCUITS ***(10 Periods)***

Introduction to analog VLSI and mixed signal issues in CMOS technologies, Trade-offs in mixed signal design, Introduction to Switched Capacitor circuits - basic building blocks, Operation and Analysis, Non-idealeffects in switched capacitor circuits, Switched capacitor integrators first order filters, Switch sharing, Biquad filters.

Module 2: PHASE LOCKED LOOP (PLL) ***(08 Periods)***

Basic PLL topology, Dynamics of simple PLL, Charge pump PLLs-Lock acquisition, Phase/Frequency detector and charge pump, Basic charge pump PLL, Non-ideal effects in PLLs-PFD/CP non-idealities, Jitter in PLLs, Delay locked loops, applications.

Module 3: DATA CONVERTER FUNDAMENTALS ***(12 Periods)***

DC and dynamic specifications, Quantization noise, performance limitations, Nyquist rate D/A converters - Decoder based Converters, Binary-Scaled converters, Thermometer-code converters, Hybrid converters.

Module 4: NYQUIST RATE A/D CONVERTERS ***(07 Periods)***

Successive approximation converters, Flash converter, Two-step A/D converters, Interpolating A/D Converters, Folding A/D converters, Pipelined A/D converters, Time-Interleaved Converters.

Module 5: OVERSAMPLING CONVERTERS ***(08 Periods)***

Noise shaping modulators, Decimating filters and interpolating filters, Higher order modulators, Delta sigma modulators with multibit quantizers, Delta sigma D/A.

Total Periods: 45

EXPERIENTIAL LEARNING

LIST OF EXERCISES:

1. Design a High Speed Comparator (Two Stage Cross Coupled Clamped Comparator, Strobed Flip-Flop) and Develop its Schematic and Layout and Assess the related Parameters.
2. Design Switched Capacitor Circuits (Parasitic Sensitive Integrator, Parasitic Insensitive integrator) and Develop its Schematic and Layout and Assess the related Parameters.
3. Design a Switched Capacitor Common Mode Feedback Amplifier and Develop its Schematic and Layout and Assess the related Parameters.
4. Design a Biquad Filter and Develop its Schematic and Layout and Assess the related Parameters.
5. Design a Phase Locked Loop and Develop its Schematic and Layout and Assess the related Parameters.
6. Design a Voltage Controlled Oscillator and Develop its Schematic and Layout and Assess the related Parameters.
7. Design a Digital Locked Loop and Develop its Schematic and Layout and Assess the related Parameters.
8. Design a Sample and Hold Circuit and Develop its Schematic and Layout and Assess the related Parameters.

9. Design Digital to Analog Converters (R-2R Ladder/ Cycic) and Develop its Schematic and Layout and Assess the related Parameters.
10. Design Analog to Digital Converters (SAR/ Over Sampling) and Develop its Schematic and Layout and Assess the related Parameters.
11. Design Higher Order Modulators and Develop its Schematic and Layout and Assess the related Parameters.
12. Design High Performance FIR Filter for Decimation and Interpolation and Develop its Schematic and Layout and Assess the related Parameters.

RESOURCES

TEXT BOOKS:

1. David A. Johns,Ken Martin, "Analog Integrated Circuit Design", Wiley Student Edition, 2nd Edition, 2013.
2. Behzad Razavi, "Design of Analog CMOS Integrated Circuit", Tata-McGrawHill, 2nd Edition 2017.
3. Philip E. Allen and Douglas R. Holberg, "CMOS Analog Circuit Design", Oxford University Press Indian 3rd Edition, 2013.

REFERENCE BOOKS:

1. Rudy Van De Plassche, "CMOS Integrated Analog-to-Digital and Digital-to-Analog converters", Springer US, 2nd Edition, 2005.
2. Richard Schreier, "Understanding Delta-Sigma Data converters", Wiley IEEE Press, 2nd Edition, 2016.
3. R. Jacob Baker, "CMOS Mixed-Signal Circuit Design", John Wiley & Sons, 2nd Edition, 2008.

SOFTWARE/TOOLS:

1. Software: Cadence/ synopsys/ mentor graphics/ DSCH and Microwind Tools/ Symica TCAD Tools

VIDEO LECTURES:

1. https://freevideolectures.com/course/3676/cmos-mixed-signal-vlsi-design
2. http://www.satishkashyap.com/2012/08/video-lectures-on-mixed-signal.html

PROGRAM ELECTIVE

Course Code	Course Title	L	T	P	S	C
22EC202015	**FPGA ARCHITECTURES**	3	-	3	-	4.5

Pre-Requisite -

COURSE DESCRIPTION: This course provides a detailed discussion and hands-on experience on Evolution of Programmable Devices, Xilinx, Actel, Altera FPGAs, Logic Synthesis, Technology Mapping, Finite State Machines, Realizations of SM Charts, One Hot Method, System level Design, Device Applications-Fast Bus Controller, FIFO Controller & Intelligent I/O Subsystem

COURSE OUTCOMES: After successful completion of the course, students will be able to:

CO1. Analyze the architectures of programmable logic devices and technology mapping issues in CPLDs and FPGAs.

CO2. Analyze various Finite state machine charts and its architectures to evaluate the performance of VLSI systems.

CO3. Understand the applications of FPGA in communications, speech processing, Image and video processing.

CO-PO Mapping Table:

Course Outcomes	Program Outcomes					
	PO1	PO2	PO3	PO4	PO5	PO6
CO1	3	-	-	-	-	-
CO2	3	-	3	-	-	-
CO3	3	-	3	-	-	-
Course Correlation Mapping	**3**	**-**	**3**	**-**	**-**	**-**

Correlation Levels: **3: High;** **2: Medium;** **1: Low**

COURSE CONTENT

Module 1: Introduction to Programmable Logic and FPGAs ***(08 Periods)***

Evolution of Programmable Devices, CPLD Altera Series Max 5000, MAX 7000 Series. Field Programmable Gate Arrays –Design Flow, Placement, Routing Architecture. Altera FPGAs. Advanced Micro Devices (AMD) FPGA. Applications of FPGAs.

Module 2: ***(09 Periods)***

Xillinx and ActelFPGAs :Case Studies – Xilinx XC2000, XilinxXC3000, Xilinx 4000 FPGAS. Actel FPGAs- Actel ACT1, Actel ACT2, Actel ACT3.

Technology Mapping for FPGAs:Logic Synthesis. Lookup Table Technology, Mapping Multiplexer Technology Mapping- The Proserphine Technology Mapper, Multiplexers Technology Mapping in Mispga, A map and XA map Technology Mappers.

Module 3 Finite State Machine ***(09 Periods)***

Finite State Machines, State Transition Table, State Assignment for FPGAs, Hazards and One Hot Encoding. Mustang. State Machine Charts, Derivations of State Machine Charges, Realization of State Machine Charts.

Module 4 FSM Architectures and System Level Design ***(10 Periods)***

Architectures CenteredAround Non Registered PLDs, State Machine Designs Centered Around Shift Registers, One – Hot Design Method, Use of ASMs in One Hot Design, Application of One Hot Method. System Level Design – Controller, Data Path and Functional Partition.

Module 5 Design Applications ***(09 Periods)***

MAX 5000 Timing, Using Expanders to Build Registered Logic in MAX EPLDs, Simulating Internal Buses in General Purpose EPLDs, Fast Bus Controllers with EPM5016, Micro Channel Bus Master and SDP Logic with the EPM5032 EPLD, FIFO Controller Using an EPM7096, Integrating an Intelligent I/O Subsystem with a Single EPM5130 EPLD.

Total Periods: 45

EXPERIENTIAL LEARNING

LIST OF EXERCISES:

VLSI Front End Design programs:

Programming can be done using any complier. Download the programs on FPGA/CPLD pattern generator (32 channels and logic analyser)/Chipscope pro apart from verification by

1. Write Verilog code for the design of 8-bit
    i. Carry Ripple Adder
    ii. Carry Look Ahead adder
    iii. Carry Skip Adder
2. Write Verilog Code for 8-bit
    i. Array Multiplication (Signed and Unsigned)
    ii. Booth Multiplication (Radix-4)

3. Write Verilog Code for 8-bit
    i. Magnitude Comparator
    ii. LFSR
    iii. Parity Generator
    iv. Universal Shift Register
4. Design a Melay and Moore Sequence Detector using Verilog to detect Sequence. Eg. 11101(with and without overlap) any sequence can be specified.

RESOURCES

TEXT BOOKS:

1. S.Brown, R.Francis, J.Rose, Z.Vransic, "Field Programmable Gate Array‖, Kluwer Publication, 1992.
2. P.K.Chan& S. Mourad, —Digital Design Using Field Programmable Gate Array‖, Prentice Hall (PTE), 1994.
3. Richard Tinder, —Engineering Digital Design‖, Academic Press, 2nd Edition, 2000.

REFERENCE BOOKS:

1. Charles H. Roth, Jr, —Fundamentals of Logic Design‖, Cengage Learning, 5th Edition, 2004.
2. S.Trimberger, Edr., "Field Programmable Gate Array Technology‖, Kluwer Academi Publications, 1994.

SOFTWARE/TOOLS:

1. Software: Xilinx ISE Suite Version, Mentor Graphics-Questa Simulator, Mentor Graphic Precision RTL.
2. Hardware: Personal Computer with necessary peripherals, configuration and operatin System and relevant VLSI (CPLD/FPGA) hardware Kits.

VIDEO LECTURES:

1. https://nptel.ac.in/courses/108101089
2. https://nptel.ac.in/courses/117108040
3. https://nptel.ac.in/courses/117103125
4. https://nptel.ac.in/courses/117106149

Web Resources:

1. https://www.xilinx.com/products/silicon-devices/fpga.html
2. https://www.eecg.utoronto.ca/~brown/papers/dac05-ling.pdf
3. https://en.wikipedia.org/wiki/Finite-state_machine
4. digitalsystemdesign.in/wp-content/uploads/2018/06/FSM-design.pdf

PROGRAM ELECTIVE

Course Code	Course Title	L	T	P	S	C
22EC201016	**PHYSICAL DESIGN AUTOMATION**	3	-	-	-	3

Pre-Requisite - Digital CMOS VLSI Design, FPGA Architectures

Anti-Requisite -

Co-Requisite -

COURSE DESCRIPTION: This course provides a detailed discussion on the design cycles, various techniques onPartitioning, Placement and Routing and addressing their problems

COURSE OUTCOMES: After successful completion of the course, students will be able to:

CO1. Demonstrate about various steps in VLSI Design cycle

CO2. Formulate CAD design using algorithmic paradigms

CO3. Apply various algorithms for floor planning, routing and Placement

CO4. Analyze physical design including partitioning and routing

CO5. Analyze physical design automation for FPGA, CPLD & MCM's

CO-PO Mapping Table:

Course Outcomes	Program Outcomes					
	PO1	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**
CO1	3	3	--	-	-	-
CO2	3	3	3	-	-	-
CO3	3	3	2	-	-	-
CO4	3	--	3	-	-	-
CO5	3	3	3	-	-	-
Course Correlation Mapping	**3**	**3**	**3**	**-**	**-**	**-**

Correlation Levels: **3: High;** **2: Medium;** **1: Low**

COURSE CONTENT

Module 1: VLSI Physical Design Automation ***(08 Periods)***

VLSI Design Cycle, New Trends in VLSI Design Cycle, Physical Design Cycle, New Trends in Physical Design Cycle, Design Styles, System Packaging Styles.

Module 2: Graph Theory and Computational Geometry ***(08 Periods)***

Basic Terminology, Basic Graph Algorithms : Graph Search Algorithms- Depth-First Search, Breadth-First Search. Spanning Tree Algorithms- Kruskal's Algorithm. Shortest Path Algorithms- Single Pair Shortest Path, All Pairs Shortest Paths Computational Geometry Algorithms- Line Sweep Method, Extended Line Sweep Method.

Module 3: Partitioning, Floor Planning, Pin Assignment and Placement ***(12 Periods)***

Partitioning – Problem formulation, Classification of Partitioning algorithms-Kernighan-Lin Algorithm, Extensions of Kernighan-Lin algorithm ,Simulated Annealing and Evolution, Metric allocation method.

Floor Planning – Problem formulation, Classification of floor planning algorithms constraint based floor planning, Rectangular Dualization. Pin Assignment – Problem formulation, Classification of pin assignment algorithms General and channel Pin assignments.

Placement – Problem formulation, Classification of placement algorithms- Partitioning based placement algorithms;

Module 4: Global Routing and Detailed Routing ***(08 Periods)***

Global Routing – Problem formulation, Classification of global routing algorithms-Maze routing algorithms, Line-Probe Algorithms, Shortest Path Based Algorithms, Steiner Tree based Algorithms **Detailed Routing** – Problem formulation, Classification of routing algorithms- Single layer routing algorithms

Module 5: Physical design Automation of FPGAs ***(09 Periods)***

Physical Design cycle for FPGAs, Partitioning, Routing – Routing Algorithm for the Non- **FPGA Technologies** Segmented model, Routing Algorithms for the Segmented Model.

MCM Technologies-Introduction to MCM Technologies, MCM Physical Design Cycle.

Total Periods: 45

EXPERIENTIAL LEARNING

1. Artificial Intelligence Algorithms and Applications in VLSI Design and Technology
2. Machine Learning Algorithms and Applications in VLSI Design and Technology

RESOURCES

TEXT BOOKS:

1. N.A.Sherwani, "Algorithms for VLSI Physical Design Automation", (3/e), Kluwer, 1999.
2. Sung-Mo Kang, Yusuf Leblebici, "CMOS Digital Integrated Circuits: Analysis and Design" TMH, 3rd Edition, 2011.

REFERENCE BOOKS:

1. Sadiq M Sait, Habib Youssef, "VLSI Physical Design Automation-Theory and Practice" Worl Scientific.
2. S. H. Gerez, "Algorithms for VLSI Design Automation", Wiley student Edition, John Wiley an Sons (Asia) Pvt. Ltd. 1999,

VIDEO LECTURES:

1. https://onlinecourses.nptel.ac.in/noc21_cs12/preview
2. https://www.digimat.in/nptel/courses/video/106105161/L01.html
3. https://archive.nptel.ac.in/courses/106/105/106105161/

Web Resources:

1. https://www.classcentral.com/course/swayam-vlsi-physical-design-7894

PROGRAM ELECTIVE

Course Code	Course Title	L	T	P	S	C
22EC202017	**MEMORY TECHNOLOGIES**	3	-	3	-	4.5

Pre-Requisite -Digital CMOS VLSI Design, IC Fabrication, VLSI Design Verification and Testing

Anti-Requisite -

Co-Requisite -

COURSE DESCRIPTION: This course provides a detailed discussion on Random access memory Technology; Non-Volatile memory designs; Reliability and Radiation effects of semiconductor memory; Packaging technologies, Fault modeling and Testing of memory.

COURSE OUTCOMES: After successful completion of the course, students will be able to:

CO1. Analyse various Random-Access Memory Technologies,Non-Volatile Memory Designs and Technologiesfor optimized memory design.

CO2. Analyse the reliability and radiation issues of semiconductor memories for different memory Architectures.

CO3. Apply advanced memory and high packaging technologiesin memory optimization.

CO4. Apply various memory fault models and appropriate testing Techniques to improve the performance of VLSI systems.

CO-PO Mapping Table:

Course Outcomes	Program Outcomes					
	PO1	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**
CO1	3	**-**	-	-	-	-
CO2	3	-	-	-	-	-
CO3	3	2	3	-	-	-
CO4	3	2	3	-	-	-
Course Correlation Mapping	**3**	**2**	**3**	-	-	-

Correlation Levels: **3: High;** **2: Medium;** **1: Low**

COURSE CONTENT

Module 1: RANDOM ACCESS MEMORY TECHNOLOGIES ***(11 Periods)***

Static Random Access Memories (SRAMs)*:*Basic SRAM Architecture and Cell Structures, High performance SRAMs, Advanced SRAM Architectures , BiCMOS SRAMs, Low-Voltage SRAMs ,SOI SRAMs,Specialty SRAMs.
Dynamic Random Access Memories (DRAMs)*:* DRAM Technology Development, CMOS DRAMs, DRAMs Cell Theory and Advanced Cell Structures, BiCMOS DRAMs,Cache DRAM, Virtual Channel Memory (VCM) DRAMs, Multilevel Storage DRAMs, SOI DRAMs , Gigabit DRAM Scaling Issues and Architectures, Advanced DRAM design and Architecture, Application Specific DRAMs.

Module 2: NON-VOLATILE MEMORY DESIGNS AND TECHNOLOGIES ***(08 Periods)***

Masked Read-Only Memories (ROMs), Programmable Read-Only Memories (PROMs),Non-volatile memory advances, Floating Gate Cell Theory and Operations, Erasable (UV) - Programmable Road-Only Memories (EPROMs), Electrically Erasable PROMs (EEPROMs), Flash Memories,Multilevel Non-volatile Memories.

Module 3: SEMICONDUCTOR MEMORY RELIABILITY AND RADIATION EFFECTS ***(09 Periods)***

Reliability**:** General Reliability Issues, RAM Failure Modes and Mechanism, Non-volatile Memory Reliability, Reliability Modeling and Failure rate Prediction, Design for Reliability, Reliability Test Structures, Reliability Screening and Qualification.
Radiation:Radiation Effects, Radiation Hardening Techniques- Radiation Hardening Process and Design Issues-Radiation Hardened Memory Characteristics, Radiation hardness assurance.

Module 4: ADVANCED MEMORY AND HIGH-DENSITY PACKING TECHNOLOGIES ***(09 Periods)***

Ferroelectric Random-Access Memories (FRAMs), Gallium Arsenide (GaAs) FRAMs, Analog Memories, Magneto resistive Random Access Memory, Experimental Memory Devices. Hybrids and MCMs (2D), Memory Stacks and MCMs (3D),Memory Cards, High Density Memory Packaging Future Directions

Module 5: MEMORY FAULT MODELING AND TESTING ***(08 Periods)***

RAM Fault Modeling, Electrical Testing, RAM Peusdo Random Testing, Megabit DRAM Testing, Nonvolatile Memory Modeling and Testing, IDDQ Fault Modeling and Testing, Application Specific Memory Testing.

Total Periods: 45

EXPERIENTIAL LEARNING

1. Develop4MB and 16MB SRAM, advanced SRAM Architectures.
2. Design and Explain the working principle of 8KB Static NVRAM..
3. Examine the testing technique used to detect and correctthe errors in memory design.
4. Illustrate high density packaging methodology on 3Dmemory stacks and MCMs.

List of Exercises:

Design,Synthesize and Implement the followinglogic circuits:

1. Single Port Synchronous RAM.

2. Synchronous FIFO.

3. UART Model.

4. Dual Port Asynchronous RAM.

5.SRAM

6.DRAM

7.PROM

8.Single Error Detection and Correction

9.Multiple Error Detection and Correction

10. Random Error Detection and Correction

11.Adacent Error Detection and Correction

12.MBIST

RESOURCES

TEXT BOOKS:

1. Ashok K Sharma, *"Advanced Semiconductor Memories: Architectures, Designs and Applications"*, Wiley Interscience,2003.
2. Ashok K Sharma,"*SemiconductorMemories:Technology*", Testing & Reliability, PHI, 2012.

REFERENCE BOOKS:

1. Kiyoo Itoh, "*VLSI memory chip design*", Springer International Edition, 2001.
2. Luecke Mize Carr, "*Semiconductor Memory design and Application*", Mc-Graw Hill, 1973

SOFTWARE /TOOLS:

Software: Xilinx ISE Suite Version, Mentor Graphics-Questa Simulator, Mentor Graphics-Precision RTL.
Hardware: Personal Computer with necessary peripherals, configuration and operating System and relevant VLSI (CPLD/FPGA) hardware Kits.

VIDEO LECTURES:

1. https://nptel.ac.in/courses/117106111/24
2. https://nptel.ac.in/courses/106105033/32
3. https://nptel.ac.in/courses/106104122/30
4. https://nptel.ac.in/courses/117101058/28

Web Resources:

1. https://researcher.watson.ibm.com/researcher/view_group.php?id=7956
2. https://www.electronics-notes.com/articles/electronic_components/semiconductor-ic-memory/memory-types-technologies.php

PROGRAM ELECTIVE

Course Code	Course Title	L	T	P	S	C
22EC203018	**RECONFIGURABLE COMPUTING**	3	-	-	4	4

Pre-Requisite - FPGA Architectures

Anti-Requisite -

Co-Requisite -

COURSE DESCRIPTION:

This course provides a detailed discussion on programming languages used in modern reconfigurable embedded systems. Topics include general-purpose computing, reconfigurable computing, and application-specific computing in digital system design, technologies of reconfigurable computing systems such as FPGAs (Field Programmable Gate Arrays), design flow and implementation in reconfigurable systems, Hardware Description Languages (HDLs) especially VHDL programming, techniques to reconfigure systems over time including partitioning and placement, and on-chip communication solutions in dynamically reconfigurable systems.

COURSE OUTCOMES: After successful completion of the course, students will be able to:

CO1. Understand the Concept of Reconfigurable Computing and FPGA Architectures.

CO2. Understand and explore the various FPGA computing platforms in terms of design tools.

CO3. Explore and apply the basic building blocks of FPGA designing in terms of Programming (HDLs).

CO4. Analyze the Coarse-grained and Fine Grain configurability for performance enhancement using multi-FPGA systems.

CO-PO Mapping Table:

Course Outcomes	Program Outcomes					
	PO1	PO2	PO3	PO4	PO5	PO6
CO1	3	-	-	-	-	-
CO2	3	-	-	-	-	-
CO3	3	-	-	-	-	-
CO4	3	-	-	-	-	-
Course Correlation Mapping	3	-	-	-	-	-

Correlation Levels: 3: High; 2: Medium; 1: Low

COURSE CONTENT

Module 1: DEVICE ARCHITECTURE ***(09 Periods)***

General Purpose Computing Vs Reconfigurable Computing – Simple Programmable Logic Devices – Complex Programmable Logic Devices – FPGAs – Device Architecture - Case Studies

Module 2: RECONFIGURABLE COMPUTING ARCHITECTURES AND SYSTEMS ***(10 Periods)***

Reconfigurable Processing Fabric Architectures – RPF Integration into Traditional Computing Systems – Reconfigurable Computing Systems – Case Studies – Reconfiguration Management.

Module 3: PROGRAMMING RECONFIGURABLE SYSTEMS ***(10 Periods)***

Compute Models - Programming FPGA Applications in HDL – Compiling C for Spatial Computing – Operating System Support for Reconfigurable Computing.

Module 4: MAPPING DESIGNS TO RECONFIGURABLE PLATFORMS ***(09 Periods)***

The Design Flow - Technology Mapping – FPGA Placement and Routing – Configuration Bitstream Generation – Case Studies with Appropriate Tools.

Module 5: APPLICATION DEVELOPMENT WITH FPGAS ***(07 Periods)***

Case Studies of FPGA Applications – System on a Programmable Chip (SoPC) Designs

Total Periods: 45

EXPERIENTIAL LEARNING

1. Illustrate the usage of reconfigurable hardware in embedded systems.
2. Design and Sketch a 16-bit reconfigurable adder and develop its architecture .

PROJECT BASED LEARNING:

1. IoT based Home automation using FPGA
2. Median Filter Design using FPGA
3. Discrete Wavelet Transform using FPGA

RESOURCES

TEXT BOOKS:

1. Reconfigurable Computing: The Theory and Practice of FPGA-Based Computation, edited b Scott Hauck and Andre DeHon, Elsevier, Inc. (Morgan Kaufmann Publishers), Amsterdam, 200
2. Christophe Bobda, ―Introduction to Reconfigurable Computing – Architectures, Algorithms an Applications‖, Springer, 2010.

REFERENCE BOOKS:

1. Maya B. Gokhale and Paul S. Graham, ―Reconfigurable Computing: Accelerating Computatio with Field-Programmable Gate Arrays‖, Springer, 2005.
2. Reconfigurable Computing: From FPGAs to Hardware/Software Codesign 2011 Edition by Joa Cardoso (Editor), Michael Hübne, Springer

VIDEO LECTURES:

1. Prof. Ken Eguro, University of Washington, Video lecture on Reconfigurable Computing Sponsored by Microsoft Research

Web Resources:

1. https://www.microsoft.com/en-us/research/video/candidate-talk-reconfigurable-computing-architectural-and-design-tool-challenges/
2. http://www.xilinx.com/
3. http://www.altera.com/

PROGRAM ELECTIVE

Course Code	Course Title	L	T	P	S	C
22EC203019	**VLSI DIGITAL SIGNAL PROCESSING**	3	-	-	4	4

Pre-Requisite – Computational Methods in Microelectronics

COURSE DESCRIPTION: This course provides a detailed description of various DSP Algorithms, Data Flow graph Representations, Iteration Bound, The Minimum Cycle Mean Algorithm, Pipelining and Parallel Processing techniques, Retiming concepts, Fast Convolution, Arithmetic Strength Reduction techniques for Filter design, Pipelining and Parallel Processing for design of IIR Filters.

COURSE OUTCOMES:

After successful completion of the course, student will be able to:

CO1. Analyze various DSP algorithms to design digital and adaptive Filter Banks for multidisciplinary environments.

CO2. Analyze iterative bound, parallel and pipelining processing methods in the frequency analysis of FIR filters.

CO3. Understand convolution methods and arithmetic strength reductions in analyzing Parallel FIR filters.

CO4. Design IIR filters by applying pipelining and parallel processing techniques.

CO5. Analyze scaling and round off noise to evaluate the performance of digital filters.

CO-PO Mapping Table:

Course Outcomes	Program Outcomes					
	PO1	PO2	PO3	PO4	PO5	PO6
CO1	3	-	-	-	-	-
CO2	3	-	-	-	-	-
CO3	2	2	-	-	-	-
CO4	2	3	3	-	-	-
CO5	3	-	3	-	-	-
Level of correlation of the course	**3**	**3**	**3**			

Correlation Levels: 3: High; 2: Medium; 1: Low

COURSE CONTENT

Module 1: INTRODUCTION TO DIGITAL SIGNAL PROCESSING (Periods: 07)
Typical DSP Algorithms – Convolution, Correlation, Digital Filters, Adaptive Filters. Representation of DSP Algorithms - Block Diagrams, Signal-Flow Graph, Data-Flow Graph.

Module 2: ITERATION BOUND, PIPELINING AND PARALLEL PROCESSING OF FIR FILTER

(Periods: 08)

Iteration Bound - Data-Flow Graph Representations, Loop Bound and Iteration Bound, Algorithms for Computing Iteration Bound-Longest Path Matrix Algorithm, The Minimum Cycle Mean Algorithm.

Pipelining and Parallel Processing - Pipelining of FIR Digital Filters. Parallel Processing, Pipelining and Parallel Processing for Low Power.

Retiming – Definitions and Properties, Solving Systems of Inequalities, Retiming Techniques.

Module 3: FAST CONVOLUTION AND ARITHMETIC STRENGTH REDUCTION IN FILTERS
(Periods: 10)

Fast Convolution - Cook-Toom Algorithm, Modified Cook-Toom Algorithm. Design of Fast Convolution Algorithm by Inspection.
Parallel FIR filters, Fast FIR algorithms - Two parallel and three parallel fast FIR algorithms. Low- Complexity FIR Filters. Parallel architectures for Rank Order filters – Odd-Even Merge-Sort architecture, Rank Order filter architectures, Parallel Rank Order filters, Running Order Merge – Sorter, Low power Rank Order filter.

Module 4: PIPELINED AND PARALLEL RECURSIVE FILTERS (Periods: 10)
Pipeline Interleaving in Digital Filters, Pipelining in 1stOrder IIR Digital Filters, Pipelining in Higher-Order IIR Digital Filters-Clustered Look-Ahead Pipelining, Stable Clustered Look-Ahead Filter Design. Parallel Processing for IIR Filters.

Module 5: SCALING AND ROUNDOFF NOISE (Periods: 10)
Scaling and Roundoff Noise, State Variable Description of Digital Filters, Scaling and Round off Noise Computation, Roundoff Noise Computation Using State Variable Description, Slow-Down, Retiming and Pipelining.

Total Periods: 45

PROJECT BASED LEARNING

1. Determine the fast algorithm ordering that will lead to the best block structure for a 72-tap FIR filter for block sizes 12 & 36 such that the sum of the number of addition and multiplication operations is minimized.

2. Consider the IIR digital filter transfer function

$$H(z) = \frac{1}{1 - \frac{4}{3}z^{-1} + \frac{5}{12}z^{-2}}$$

Obtain an equivalent 4-level pipelined transfer function using Clustered look-ahead.

RESOURCES

TEXT BOOKS:

1. KeshabK.Parhi, "VLSI Digital Signal Processing Systems, Design and Implementation", John Wiley, Indian Reprint, 2007.

REFERENCE BOOKS:

1. U. Meyer – Baese, "Digital Signal Processing with Field Programmable Arrays", Springer, Second Edition, Indian Reprint, 2007

2. George A. Constantinides, Peter Y.K. Cheung, Wayne Luk, "Synthesis and Optimization of DSP Algorithms", Kluwer Academic Publishers,2004.

VIDEO LECTURES:

1. https://www.coursera.org/learn/dsp1
2. https://programs.online/free-online-programs/p/nptel/vlsi-signal-processing-online
3. https://onlinecourses.nptel.ac.in/noc20_ee44/preview

Web Resources:

1. https://docs.google.com/viewer?a=v&pid=sites&srcid=ZGVmYXVsdGRvbWFpbnxwZXJzb25h bHdlYnBhZ2VvZnByb2ZzdXJlc2h8Z3g6NTkwZjFiMzRlZjQyNzE2NA
2. https://doku.pub/documents/vlsi-digital-signal-processing-keshab-k-parhi-7l5r8yk677qk

PROGRAM ELECTIVE

Course Code	Course Title	L	T	P	S	C
22EC201020	**ELECTROMAGNETIC INTERFERENCE AND COMPATIBILITY**	3	-	-	-	3

Pre-Requisite -

Anti-Requisite -

Co-Requisite -

COURSE DESCRIPTION:

This course provides theoretical, analytical and practical information required to understand EMI/C with respect to aspects viz. various sources of EMI, their characterizations and measurement procedures, tools and techniques for achieving electromagnetic compatibility.

COURSE OUTCOMES: After successful completion of the course, students will be able to:

CO1. Analyze the concepts of EMI/C and non-ideal behaviour of components.

CO2. Apply standards and regulations for measuring radiated and conducted interferences in open area test sites.

CO3. Apply the practices of grounding, shielding and electrical bonding to avoid or reduce EMI/C.

CO4. Analyze various EMC filters, connectors and components.

CO-PO Mapping Table:

Course Outcomes	Program Outcomes					
	PO1	PO2	PO3	PO4	PO5	PO6
CO1	3	-	-	-	-	-
CO2	3	2	2	-	-	-
CO3	3	2	2	-	-	-
CO4	3	2	2	-	-	-
Course Correlation Mapping	**3**	**2**	**2**	**-**	**-**	**-**

Correlation Levels: 3: High; 2: Medium; 1: Low

COURSE CONTENT

Module 1: INTRODUCTION TO EMI/C AND COMPONENTS NON-IDEALITY ***(10 Periods)***

Introduction to EMI/C: Concepts and Definition of EMI and EMC, Natural and nuclear EMI sources. Radiated and Conducted Emissions.
Components non-ideality: Wires, printed circuit board (PCB) lands, effect of component leads, resistors, capacitors, inductors.

Module 2: EMI/EMC STANDARDS AND OPEN AREA TEST SITES ***(08 Periods)***

EMI/EMC Standards - Introduction, Standards for EMI/EMC, MIL STD - 461/462, IEEE/AXSI Standards, FCC regulations.

Open Area Test Sites - open area test site measurements, Measurement precautions, open area test site, Terrain Roughness, Measurement of test site imperfections, Antenna factor measurement, Measurement errors.

Module 3: RADIATED INTERFERENCE AND CONDUCTED INTERFERENCE MEASUREMENTS ***(09 Periods)***

Radiated Interference measurements - Anechoic chamber, Transverse Electromagnetic Cell, Reverberating chamber, Basic overview of GTEM Cell, Comparison of test facilities.

Conducted Interference measurements - Characterization of conduction currents/voltages, Conducted EM noise on power supply lines, Immunity to conducted EMI, Detectors and measurement.

Module 4: GROUNDING, SHIELDING AND BONDING ***(09 Periods)***

Grounding - Principles and Practice of Earthing, Precautions in Earthing, Measurements of ground resistance, Cable shield Grounding.

Shielding - Shielding Theory, Shielding Materials, Shielding Integrity at discontinuities, Conductive coatings, Cable shielding.

Electrical Bonding.

Module 5: EMC FILTERS, CONNECTORS AND COMPONENTS ***(09 Periods)***

Characteristics and Types of Filters - Impedance Mismatch Effects, Lumped Element Low Pass Filter, High Pass Filter, Band Pass Filter, Band Reject filter. Power Line filter Design - Common mode filter, Differential mode filter, Combined CM and DM filter.

EMC Connectors - Pigtail Effect.

EMC Components – EMC Gaskets, Isolation transformers. Opto Isolators.

Total Periods: 45

EXPERIENTIAL LEARNING

1. Demonstrate an experiment to understand how an electrically conductive surface in physical contact with a charged dielectric can be inconspicuously charged to very high voltages.
2. Demonstrate an experiment to understand the concepts of self and mutual inductance and capacitance.
3. Demonstrate an experiment to understand the mechanism of crosstalk in cables.

RESOURCES

TEXT BOOKS:

1. Clayton R. Paul, "Introduction to Electromagnetic Compatibility", Wiley Student Edition, 2018
2. V. Prasad Kodali, "Engineering Electromagnetic Compatibility", Wiley-IEEE Press, 2nd Edition 2001.

REFERENCE BOOKS:

1. Christos Christopoulos, "Principles and Techniques of Electromagnetic Compatibility", CRC Press, 3rd edition, 2022.

VIDEO LECTURES:

1. https://nptel.ac.in/courses/108106138
4. https://www.coursera.org/lecture/inputfilterdesign/introduction-to-electromagnetic-compatibility-emc-and-interference-emi-762O3

Web Resources:

1. https://www.egr.msu.edu/emrg/electromagnetic-compatibility-emc-course-notes
3. http://wireless.ictp.it/school_2004/lectures/struzak/Introd_to_EMC.pdf
4. https://www.montana.edu/tjkaiser/ee335/notes/EE335-29-EMI.pdf

PROGRAM ELECTIVE

Course Code	Course Title	L	T	P	S	C
22EC201021	**FAULT TOLERANT AND DEPENDABLE SYSTEMS**	3	-	-	-	3

Pre-Requisite Embedded System Design

Anti-Requisite --

Co-Requisite --

COURSE DESCRIPTION:

This course provides a detailed discussion on Fault Tolerance; Dependability Characteristics; Hardware Redundancy; Information, Time and Software Redundancy.

COURSE OUTCOMES: After successful completion of the course, students will be able to:

CO1. Analyze various faults by understanding threats to system dependability and fault tolerant techniques.

CO2. Evaluate various characteristics of dependability in digital systems.

CO3. Analyze system dependability using various hardware redundancy approaches to design fault tolerant hardware systems.

CO4. Apply various codes and time redundancy techniques to improve system dependability.

CO5. Analyze various approaches for the design of fault tolerant software systems

CO-PO Mapping Table:

Course Outcomes	Program Outcomes					
	PO1	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**
CO1	3	-	2	-	-	-
CO2	3	-	2	-	-	-
CO3	3	-	3	-	-	-
CO4	3	1	3	-	-	-
CO5	3	1	-	-	-	-
Course Correlation Mapping	**3**	**1**	2.5	**-**	**-**	**-**

Correlation Levels: **3: High;** **2: Medium;** **1: Low**

COURSE CONTENT

Module 1: FAULT TOLERANCE (09 Periods)

Fault Classification; Types of Redundancy; Measures of Fault Tolerance: Traditional and Network; Importance of Fault Tolerance in dependable System design.

Module 2: DEPENDABILITY CHARACTERISTICS (09 Periods)

Dependability attributes: Reliability, Availability and Safety; Dependability impairments; Dependability Means: Fault Tolerance, Prevention, Removal and Forecasting.

Module 3: HARDWARE REDUNDANCY (09 Periods)

Redundancy Allocation; Passive Redundancy: Triple and NMR; Active Redundancy: Duplication with Comparison, Stand by Redundancy, Pair A Spare; Hybrid Redundancy: Self Purging, NMR with Spares, Byzantine Failures.

Module 4: INFORMATION AND TIME REDUNDANCY (09 Periods)

Information Redundancy: Notion, Parity Codes, Linear Codes, Cyclic Codes, Unordered and Arithmetic Codes.

Time Redundancy: Transient and Permanent Faults

Module 5: SOFTWARE REDUNDANCY (09 Periods)

Software VS. Hardware; Single Version Techniques: Fault detection, containment & Recovery Techniques; Multi Version Techniques: Recovery Block, N- Version Programming, N Self-Checking Programming, Importance of Design Diversity; Software Testing.

Total Periods: *45*

Topics for self-study are provided in the lesson plan.

EXPERIENTIAL LEARNING

LIST OF EXERCISES:

1. Emphasize on fault tolerant processor architectural design issues
2. Survey on dependability evaluation techniques such as Fault trees & Markov Chains
3. Distributed Systems need specified fault tolerant techniques – survey on the reported schemes in the literature
4. Investigate on Testing and Built-in-Self-Test Functional testing for VLSI circuits
5. Survey on Hierarchical Modelling and Analysis Package (HIMAP), developed at the IOWA STATE University to analyze reliability and availability of the systems

TEXT BOOKS:

1. Israel Koren, C. Mani Krishna, *Fault-Tolerant Systems*, Elsevier Science Publication. 2nd Edition, Sep. 2020,
2. Elena Dubrova, *Fault-Tolerant Design,* Springer, Sweden, 2013.

REFERENCE BOOKS:

1. C.M. Krishna, Kang G Shin, *Real Time Systems*, McGraw-Hill Education (India) Pvt Limited, 2010.
2. Alessandro Birolini, *Reliability Engineering: Theory and Practice*, Springer-Verlag Berlin Heidelberg, Spain. 8th ed., 2017.

ADDITIONAL LEARNING RESOURCES:

1. https://www.mdu.se/en/malardalen-university/education/further-training/ai-and-software-development/design-of-dependable-and-fault-tolerant-embedded-systems
2. https://extendedstudies.ucsd.edu/courses-and-programs/fault-tolerant-systems

PROGRAM ELECTIVE

Course Code	Course Title	L	T	P	S	C
22EC201022	COMMUNICATION BUSES AND INTERFACES	3	-	-	-	3

Pre-Requisite - Embedded Systems Design

Anti-Requisite -

Co-Requisite -

COURSE DESCRIPTION: This course provides a detailed discussion on Serial Busses, RS232 – Limitations and Applications, CAN Protocol, USB – Types, Architecture, Serial Communication Protocol using Physical Medium.

COURSE OUTCOMES: After successful completion of the course, students will be able to:

CO1. Understand the features of various serial protocols for high-speed data communication between ICs in a Board.

CO2. Analyze the limitations of RS232 to solve the problems in various communicating devices.

CO3. Develop the architecture of Controller Area Network for Application layer communication.

CO4. Apply PCIe hardware Protocol for high-speed communication between compatible devices.

CO5. Apply appropriate serial communication protocols and USB transfer types forhigh performance communication bus.

CO-PO Mapping Table:

Course Outcomes	Program Outcomes					
	PO1	PO2	PO3	PO4	PO5	PO6
CO1	3	-	-	-	-	-
CO2	3	-	-	-	-	-
CO3	3	3	-	-	-	-
CO4	3	-	-	-	-	-
CO5	3	-	-	-	-	-
Course Correlation Mapping	3	-	-	-	-	-

Correlation Levels: 3: High; 2: Medium; 1: Low

COURSE CONTENT

Module 1: Serial Bus ***(08 Periods)***

Physical interface, Data and Control signals, features

Module 2: Introduction to Serial standards ***(07 Periods)***

Limitations and applications of RS232, RS485, I2C, SPI

Module 3: Controller Area Network ***(10 Periods)***

CAN - Architecture, Data transmission, Layers, Frame formats, applications

Module 4: Introduction To PCIe ***(11 Periods)***

PCIe - Revisions, Configuration space, Hardware protocols, applications

Module 5: Universal Serial Bus ***(09 Periods)***

USB - Transfer types, enumeration, Descriptor types and contents, Device driver.
Data Streaming Serial Communication Protocol - Serial Front Panel Data Port (SFPDP) using fiber optic and copper cable

Total Periods: 45

EXPERIENTIAL LEARNING

1. Literature survey in the area of Communication Buses And Interfaces

RESOURCES

TEXT BOOKS:

1. Jan Axelson, *"Serial Port Complete - COM Ports, USB Virtual Com Ports, and Port forEmbedded Systems"*, Lakeview Research, 2nd Edition.
2. Marco Di Natale, Haibo Zeng, Paolo Giusto, Arkadeb Ghosal, "*Understanding and Using the Controller Area Network Communication Protocol: Theory and Practice*" Springer Science & Business Media, 2012.

REFERENCE BOOKS:

1. Wilfried Voss, "*A Comprehensible Guide to Controller Area Network*", Copperhill Media Corporation, 2nd Edition, 2005.
2. Jan Axelson, "*USB Complete*", Penram Publications.
3. Mike Jackson, Ravi Budruk, "*PCI Express Technology*", Mindshare Press

VIDEO LECTURES:

1. https://nptel.ac.in/courses/108102045/17
2. https://nptel.ac.in/courses/117106111/36
3. https://nptel.ac.in/courses/117104072/26
4. https://nptel.ac.in/courses/108107029/65

PROGRAM ELECTIVE

Course Code	Course Title	L	T	P	S	C
22EC201023	**CO DESIGN**	3	-	-	-	3

Pre-Requisite Advanced Computer Architecture and Embedded System Design

Anti-Requisite System On Chip

Co-Requisite -

COURSE DESCRIPTION: This course provides a detailed discussion on Issues and Algorithms in CO- Design; Prototyping and its Emulation on Target Architectures; Compilation Techniques; Design Specification; Verification Tools for Embedded Processor Architectures; System- Level Languages with its Specification and Design.

COURSE OUTCOMES: After successful completion of the course, students will be able to:

CO1. Analyze Co-Synthesis Algorithms for Co-Design Architectures.

CO2. Analyze Prototyping and emulation for specialized target architectures to system design.

CO3. Analyze target architectures in designing data-dominated and control-dominated embedded systems.

CO4. Use compilation techniques and tools for embedded processor architectures and perform verification of co-design computational models.

CO5. Apply language support for system level specification, co-simulation design and partitioning concepts in Cosyma and Lycos systems

CO-PO Mapping Table:

Course Outcomes	Program Outcomes					
	PO1	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**
CO1	3	2	-	-	-	-
CO2	3	2	-	-	-	-
CO3	3	2	-	-	-	-
CO4	3	2	3	-	-	-
CO5	3	-	3	-	-	-
Course Correlation Mapping	**3**	**2**	**3**	**-**	**-**	**-**

Correlation Levels: **3: High;** **2: Medium;** **1: Low**

COURSE CONTENT

Module 1: ***(11 Periods)***

CO-DESIGN ISSUES: Co- Design Models, Architectures, Languages, a Generic Co-design Methodology.

CO-SYNTHESIS ALGORITHMS: Hardware Software Synthesis Algorithms: Hardware-Software Partitioning, Distributed System Co-Synthesis.

Module 2: ***(10 Periods)***

PROTOTYPING AND EMULATION: Prototyping and Emulation Techniques, Prototyping and Emulation Environments, Future Developments in Emulation and Prototyping.
TARGET ARCHITECTURES: Architecture Specialization Techniques, System Communication Infrastructure, Target Architecture and Application System Classes, Architecture for Control Dominated Systems (8051-Architectures for High Performance Control), Architecture for Data Dominated Systems (ADSP21060, TMS320C60), Mixed Systems.

Module 3 ***(06 Periods)***

COMPILATION TECHNIQUES AND TOOLS FOR EMBEDDED PROCESSOR ARCHITECTURES: Modern Embedded Architectures, Embedded Software Development Needs, Compilation Technologies, Practical Consideration in a Compiler Development Environment.

Module 4 ***(07 Periods)***

DESIGN SPECIFICATION AND VERIFICATION: Design, Co-Design, the Co-Design Computational Model, Concurrency Coordinating Concurrent Computations, Interfacing Components, Design Verification, Implementation Verification, Verification Tools and Interface Verification

Module 5 ***(11 Periods)***

LANGUAGES FOR SYSTEM- LEVEL SPECIFICATION AND DESIGN-I: System – Level Specification, Design Representation for System Level Synthesis, System Level Specification Languages
LANGUAGES FOR SYSTEM-LEVEL SPECIFICATION AND DESIGN-II: Heterogeneous Specifications and Multi Language Co-Simulation, the Cosyma System and Lycos System.

Total Periods: 45

EXPERIENTIAL LEARNING

1. Check list to choose a target architecture for an application
2. Case study on requirement and specification phases in design
3. Investigation on codesign tools – commercial vs open source
4. Case study on Cosyma and Lycos systems

RESOURCES

TEXT BOOKS:

1. Jorgen Staunstrup, Wayne Wolf,"Hardware / Software Co- Design Principles and Practice" Springer, 2009.
2. Kluwer, "Hardware / Software Co- Design Principles and Practice", Academic Publishers 2002.

REFERENCE BOOKS:

1. Patrick R. Schaumont, "A Practical Introduction to Hardware/Software Co-design", Springer 2010.
2. Giovanni, Wayne Wolf, "Readings in Hardware Software Co – design", Academic Press, 2002

VIDEO LECTURES:

1. https://nptel.ac.in/courses/108102045/30
2. https://nptel.ac.in/courses/106/105/106105165/
3. https://www.coursera.org/learn/introduction-embedded-systems

Web Resources:

1. https://www.tec.ee.ethz.ch/education/lectures/hardware-software-codesign.html
2. https://ieeexplore.ieee.org/document/7525779
3. http://ptolemy.eecs.berkeley.edu/ptolemyII/ptII10.0/ptII10.0.1_20141217/ptolemy/domai s ontinuous/doc/index.htm

PROGRAM ELECTIVE

Course Code	Course Title	L	T	P	S	C
22EC202024	**REAL TIME SYSTEMS**	3	-	3	-	4.5

Pre-Requisite --Embedded Systems Design

Anti-Requisite --

Co-Requisite --

COURSE DESCRIPTION:

This course provides a detailed discussion and hands-on experience on Real Time Systems, Real Time Scheduling, Scheduling Real Time Tasks in Multiprocessor and Distributed Systems, Operating Systems Concepts and Trends in OS Design.

COURSE OUTCOMES: After successful completion of the course, students will be able to:

CO1. Analyze Real Time System Reference Model to derive efficient constrained RT applications.

CO2. Analyze various scheduling approaches to maximize resource utilization under imposed constraints.

CO3. Analyze strategies to schedule RT workload in multiprocessing and distributed RT implementations.

CO4. Analyze modern operating systems concepts to choose an efficient OS in RT system designs

CO5. Evaluate Android and Windows8 RTOS and investigate recent trends in OS Design context.

CO-PO Mapping Table:

Course Outcomes	Program Outcomes					
	PO1	PO2	PO3	PO4	PO5	PO6
CO1	3	-	2	1	-	-
CO2	3	-	2	1	-	-
CO3	3	-	3	1	-	-
CO4	3	1	3	-	-	-
CO5	3	1	-	2	-	-
Course Correlation Mapping	**3**	**1**	**2**	**1**	**-**	**-**

Correlation Levels: 3: High; 2: Medium; 1: Low

COURSE CONTENT

Module 1: REAL TIME SYSTEMS (09 Periods)

Hard Vs Soft Real Time Systems, a Reference Model of Real Time Systems: Processors and Resources, Temporal Parameters of Real Time Workload, Periodic Task Model, Precedence Constraints and Data Dependency; Functional Parameters, Resource Parameters of Jobs and Parameters of Resources, Scheduling hierarchy.

Module 2: REAL TIME SCHEDULING (09 Periods)

Clock Driven, Weighted Round Robin, Priority Driven, Dynamic Vs Static Systems, Effective Release Times and Dead Lines, Optimality and Non-optimality of EDF and LST algorithms, Challenges in Validating Timing Constraints in Priority Driven Systems, Offline Vs Online Scheduling.

Module 3: SCHEDULING REAL TIME TASKS IN MULTIPROCESSOR AND DISTRIBUTED SYSTEMS (09 Periods)

Multiprocessor task allocation, Dynamic allocation of tasks, Fault tolerant scheduling of tasks, Clocks in distributed Real Time Systems.

Module 4: OPERATING SYSTEM CONCEPTS (09 Periods)

Overview- Threads and Tasks, the Kernel; Time Services and Scheduling Mechanisms, Basic Operating System Functions: Communication and Synchronization, Event Notification and Software Interrupt Memory Management, I/O and Networking. Processor Reserves and Resource Kernel, Capabilities of Commercial Real Time Operating Systems.

Module 5: TRENDS IN OPERATING SYSTEMS DESIGN (09 Periods)

Case studies: ANDROID OS, Windows 8. **OS Design:** Problem, Interface Design, Implementation, Performance, Project Management, Trends.

Total Periods: *45*

Topics for self-study are provided in the lesson plan.

EXPERIENTIAL LEARNING

LIST OF EXERCISES:

1. Scheduling Tools Overview: TORSCHE, TIMES, CHEDDAR (2 Slot)
2. Modeling Scheduling Problem: Define Set of Tasks, Define Scheduling Problem, Run Scheduling Algorithm (2 Slot)
3. Workload (Periodic Task): Modeling Graphical Representation of Task Parameters (2 Slot)
4. Implement List Scheduling for constrained RT workload (2 Slot)
5. Implement Cyclic Scheduling for constrained RT Workload (2 Slot)
6. Real Time Scheduling: Fixed Priority Scheduling and its response time analysis (2 Slot)

SOFTWARE / TOOLS:

1. VisSim/Embedded Controls Developer (VisSim/ECD)
2. C2000 and MSP430 digital microcontroller chips from Texas Instruments.
3. TORSCHE Scheduling Toolbox with Matlab

REFERENCES:

1. VisSim Embedded Controls Developer user guide
2. http://rtime.felk.cvut.cz/scheduling-toolbox/manual/

TEXT BOOKS:

1. Jane W.S. Liu, *Real Time Systems*, Pearson Education, I Edition, April 2000.
2. Rajib Mall, *Real Time Systems-Theory and Practice*, Pearson Education India, I Edition, Nov.2012.
3. Andrew S. Tanenbaum, Herbert Bos, *Modern Operating Systems*, Pearson Education Limited, Fourth Edition, 2015.

REFERENCE BOOKS:

1. Phillip A. Laplante and Seppo J. Ovaska, *Real-Time Systems Design and Analysis: Tools for the Practitioner*, Wiley-IEEE Press, 4th edition, Nov. 2011.
2. Hermann Kopetz, Real-Time Systems: Design Principles for Distributed Embedded Applications, Springer; 2nd Edition, 2011.

ADDITIONAL LEARNING RESOURCES:

1. https://nptel.ac.in/courses/106105036
2. https://onlinecourses.nptel.ac.in/noc20_cs16/

PROGRAM ELECTIVE

Course Code	Course Title	L	T	P	S	C
22EC203025	**ADVANCED EMBEDDED SYSTEMS**	3	-	-	4	4

Pre-Requisite --Embedded System Design

Anti-Requisite --

Co-Requisite --

COURSE DESCRIPTION: This course provides a detailed discussion on hardware components, Hardware software co-design and firmware design approaches, Architectural features of PIC18 memory map, interrupts and exceptions, Program PIC18 using the various instructions, for different applications.

COURSE OUTCOMES: After successful completion of the course, students will be able to:

CO1. Understand the basic hardware components and their selection method based on the characteristics and attributes of an embedded system.

CO2. Explain the hardware software co-design and firmware design approaches.

CO3. Analyze PIC18 Architecture and Instruction Set to develop computing applications.

CO4. Develop Programs for PIC18 using ports, timers and associated on Chip resources for Specified Applications.

CO5. Design microcomputer based systems with the knowledge of Interfaces and Peripherals of PIC18 to Solve various engineering problems.

CO-PO Mapping Table:

Course Outcomes	Program Outcomes					
	PO1	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**
CO1	3	1	-	-	-	-
CO2	3	3	-	-	-	-
CO3	3	3	-	-	-	-
CO4	3	2	3	-	-	-
CO5	3	2	3	1	-	-
Course Correlation Mapping	**3**	**2**	**3**	**1**	**-**	**-**

Correlation Levels: 3: High; 2: Medium; 1: Low

COURSE CONTENT

Module 1: Embedded System ***(09 Periods)***

Embedded vs General computing system, classification, application and purpose of ES. Core of an Embedded System, Memory, Sensors, Actuators, LED, Opto coupler, Communication Interface, Reset circuits, RTC, WDT, Characteristics and Quality Attributes of Embedded Systems.

Module 2: Hardware software co-design and Firmware design ***(09 Periods)***

Hardware Software Co-Design, embedded firmware design approaches, computational models, embedded firmware development languages, Integration and testing of Embedded Hardware and firmware, Components in embedded system development environment (IDE), Files generated during compilation, simulators, emulators and debugging.

Module 3: PIC Microcontroller ***(09 Periods)***

Pin description of PIC18F452 Microcontroller, Architecture of PIC18, register organisation, Memory organisation, Data formatives & Directives, Addressing modes.

Module 4: PIC18 Peripherals ***(09 Periods)***

Instruction set, Basic port structure, Pin description of PIC18F452, Basic Port Structure, I/O port programming; Macros and modules, Structure of Timer 0 & its Programming using Assembly and C, Counter programming, Structure of timers 1, 2 and 3 & their Programming. Basics of communication – Serial/Parallel, RS232 & PIC18 connection to RS232, Serial Port Structure & programming; PIC18 interrupts, Programming timer interrupts, Programming serial interrupts.

Module 5: PIC Interrupts and Interfacing ***(09 Periods)***

Basics of interrupts, CCP,7 segment LED and LCD interfacing, keyboard interfacing, interfacing ADC, DAC, Interfacing DC motor, stepper motor, PWM using CCP.

Total Periods: 45

PROJECT BASED LEARNING:

1. Design a wireless MultiMeter using PIC18F452 Microcontroller.
2. Design a Automatic School Bell system that triggers a bell at predefined time.
3. Using Proteus simulate PWM code for PIC18F452.

RESOURCES

TEXT BOOKS:

1. K. V. Shibu, *Introduction to embedded systems*, TMH education Pvt. Ltd. 2009.
2. Muhammad Ali Mazidi, Rolin D. McKinlay, Danny causey, *PIC Microcontroller and Embedde Systems: Using C and PIC18*, Pearson Education, 2015.

REFERENCE BOOKS:

1. Raj Kamal, *Embedded systems*, McGraw Hill Education, Third Edition, 2017
2. Ramesh S. Gaonkar, *Fundamentals of Microcontrollers and Applications in Embedde Systems (With PIC18 Microcontroller Family)*, Penram International, 2010.
3. M Rafiquzzaman, Microcontroller Theory And Applications With The PIC, Wiley Indi Publications, March 2014

VIDEO LECTURES:

1. https://www.udemy.com/course/basics-of-pic18-microcontroller/?src=sac&kw=BASICS+OF+PIC18
2. https://www.udemy.com/course/introduction-to-pic18f-microcontroller/?src=sac&kw=PIC18

Web Resources:

1. http://www.ciebookstore.com/Content/Images/uploaded/PIC18-Study-GuideCIE.pdf
2. https://www.electronicwings.com/pic/getting-started-with-pic18f4550-and-mplabx-ide

UNIVERSITY ELECTIVE

Course Code	Course Title	L	T	P	S	C
22AI201701	**BUSINESS ANALYTICS**	3	-	-	-	3

Pre-Requisite -

Anti-Requisite -

Co-Requisite -

COURSE DESCRIPTION: This course emphasizes on the basic concepts of Business Analytics. It covers the basic excel skills, Excel look up functions for database queries in business analytics. By the end of this course students will acquire basic knowledge to implement statistical methods for performing descriptive, predictive and prescriptive analytics.

COURSE OUTCOMES: After successful completion of the course, students will be able to:

CO1. Understand the basic concepts and models of Business Analytics

CO2. Select Suitable basic excel function to perform analytics on spread sheets.

CO3. Apply different statistical techniques and distributions for modeling the data

CO4. Develop user-friendly Excel applications by using statistical models for effectiveness decision making.

CO5. Analyze the performance of different optimization models used in prescriptive analytics on Binary and Categorical data.

CO-PO-PSO Mapping Table:

Course Outcomes	Program Outcomes								
	PO1	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**	**PO7**	**PO8**	**PO9**
CO1	2	1	-	-	-	-	-	-	-
CO2	2	3	-	-	-	-	-	-	-
CO3	2	2	-	-	3	-	-	-	-
CO4	1	1	-	-	-	-	-	-	3
CO5	-	-	-	-	-	-	-	-	-
Course Correlation Mapping	**2**	**2**	**3**	**-**	**3**	**-**	**-**	**-**	**3**

Correlation Levels: ***3: High;*** ***2: Medium;*** ***1: Low***

COURSE CONTENT

Module 1: FOUNDATIONS OF BUSINESS ANALYTICS ***(9 Periods)***

Introduction, What is Business Analytics, Evolution of Business Analytics, Scope of Business Analytics, Data for Business Analytics, Applications of Business Analytics, Models in Business Analytics, Problem Solving with Analytics.

Module 2: ANALYTICS ON SPREADSHEETS ***(9 Periods)***

Basic Excel Skills, Excel Functions, Using Excel Lookup Functions for Database Queries, Spreadsheet Add-Ins for Business Analytics.
Visualizing and Exploring Data: Data Visualization, Creating Charts In Microsoft Excel, Other Excel Data Visualization, Statistical Methods For Summarizing Data, Exploring Data Using Pivot tables.

Module 3: DATA MODELING ***(9Periods)***

Basic concepts of Probability, Random Variables and Probability Distributions, Continuous Probability Distributions.
Statistical Sampling, Estimation population parameters, Sampling Error, Sampling Distributions, Hypothesis Testing, ANOVA, Chi Square Test.

Module 4: Predictive analytics ***(9 Periods)***

Trend lines And Regression Analysis, Modeling Relationships And Trends In Data, Simple Linear Regression, Multiple Linear Regression, Building Good Regression Models,
Strategies for predictive decision modeling, implementing models on spreadsheets, spreadsheet applications in business analytics, developing user-friendly excel applications, analysing uncertainty and model assumptions, model analysis using analytic solver platform

Module 5: Prescriptive analytics ***(9Periods)***

Linear Models: Building Linear Models, Implementing Linear Optimization Models On Spreadsheets, Graphical Interpretation Of Linear Optimization, Linear Optimization Models for prediction and Insight.
Integer Models: Solving models with Integer Variables, Integer Optimization Models with Binary Numbers
Decision Analysis: Formulating Decision Problems, Decision Strategies Without Outcome Probabilities, Decision Trees With Outcome Probabilities, Decision Trees.

Total Periods: 45

EXPERIENTIAL LEARNING

1. **Diabetic Prediction:**
   The National Institute of Diabetes and Digestive and Kidney Diseases has a created a dataset. The objective of the dataset is to diagnostically predict whether or not a patient has diabetes, based on certain diagnostic measurements included in the dataset. Several constraints were placed on the selection of these instances from a larger database. In particular, all patients here are females at least 21 years old of Pima Indian heritage. The datasets consists of several medical predictor variables and one target variable, Outcome. Predictor variables includes the number of pregnancies the patient has had, their BMI, insulin level, age, and so on. Build a machine learning model to accurately predict whether or not the patients in the dataset have diabetes or not?
2. Solve the house price prediction problem using **Linear regression analysis** method. Optimize the parameters of the regression function using gradient descent method.
3. Visualize the decision tree built for solving Heart disease prediction problem and measure the impurity of nodes created via **Decision Tree Analysis**.
   Dataset:https://www.kaggle.com/arviinndn/heart-disease-prediction-uci dataset/data
4. The data set baby boom (Using R) contains data on the births of 44 children in a one-day period at a Brisbane, Australia, hospital. Compute the skew of the wt variable, which records birth weight. Is this variable reasonably symmetric or skewed?
5. Visualize the **Distribution of data** with different feature scaling methods on online news popularity dataset for article word count.
   Dataset:https://www.kaggle.com/datasets/deepakshende/onlinenewspopularity

6. **Human Activity Recognition System:**
   The human activity recognition system is a classifier model that can identify human fitness activities. To develop this system, you have to use a smart phone dataset, which contains the fitness activity of 30 people which is captured through smart phones. This system will help you to understand the solving procedure of the **Multi-classification problem**.

RESOURCES

TEXT BOOKS:

1. James Evans, *Business Analytics*, Pearson Education, 2nd Edition, 2017.

REFERENCE BOOKS:

1. Marc J.Schniederjans, *Business Analytics*, Pearson Education,2015
2. Camm,Cochran, *Essentials of Business Analytics*, Cenage learning, 2015

VIDEO LECTURES:

1. https://nptel.ac.in/courses/110105089
2. https://archive.nptel.ac.in/courses/110/107/110107092/
3. https://nptel.ac.in/courses/110106050

Web Resources:

1. https://www.proschoolonline.com/certification-business-analytics-course/what-is-ba
2. https://michael.hahsler.net/SMU/EMIS3309/slides/Evans_Analytics2e_ppt_01.pdf
3. https://www.guru99.com/business-analyst-tutorial-course.html

UNIVERSITY ELECTIVE

Course Code	Course Title	L	T	P	S	C
22CM201701	COST MANAGEMENT OF ENGINEERING PROJECTS	3	-	-	-	3

Pre-Requisite -

Anti-Requisite -

Co-Requisite -

COURSE DESCRIPTION: This course will provide an understanding of the cost tools and techniques that can be used throughout a project's design and development. The students will be exposed to the methods, processes, and tools needed to conduct economic analysis, estimation of Project.

COURSE OUTCOMES: After successful completion of the course, students will be able to:

CO1 Understand the costing concepts and their role in decision-making.
CO2 Understand the project management concepts and their various aspects in selection.
CO3 Interpret costing concepts with project execution.
CO4 Knowledge of costing techniques in the service sector and various budgetary control techniques.
CO5 Become familiar with quantitative techniques in cost management.

CO-PO Mapping Table:

Course Outcomes	Program Outcomes					
	PO1	PO2	PO3	PO4	PO5	PO6
CO1	-	-	-	-	-	2
CO2	-	-	-	-	-	2
CO3	-	-	-	-	-	2
CO4	-	-	-	-	-	2
CO5	-	-	-	-	-	2
Course Correlation Level	-	-	-	-	-	2

Correlation Levels: 3: High; 2: Medium; 1: Low

COURSE CONTENT

Module 1: INTRODUCTION TO COSTING CONCEPTS ***(05 Periods)***

Objectives of a Costing System; Cost concepts in decision-making; Relevant cost, Differential cost, Incremental cost, and Opportunity cost; Creation of a Database for operational control.

Module 2: INTRODUCTION TO PROJECT MANAGEMENT ***(10 Periods)***

Project: meaning, Different types, why to manage, cost overruns centers, various stages of project execution: conception to commissioning. Project execution as conglomeration of technical and nontechnical activities, Detailed Engineering activities, Pre-project execution main clearances and documents, Project team: Role of each member, Importance Project site: Data required with significance, Project contracts

Module 3: PROJECT EXECUTION AND COSTING CONCEPTS ***(10 Periods)***

Project execution Project cost control, Bar charts and Network diagram, Project commissioning: mechanical and process, Cost Behavior and Profit Planning Marginal Costing; Distinction between Marginal Costing and Absorption Costing; Break-even Analysis, Cost-Volume-Profit Analysis, Various decision-making problems, Pricing strategies: Pareto Analysis, Target costing, Life Cycle Costing

Module 4: COSTING OF SERVICE SECTOR AND BUDGETARY CONTROL ***(10 Periods)***

Just-in-time approach, Material Requirement Planning, Enterprise Resource Planning, Activity Based Cost Management, Bench Marking; Balanced Score Card and Value-Chain Analysis, Budgetary Control: Flexible Budgets; Performance budgets; Zero-based budgets

Module 5: QUANTITATIVE TECHNIQUES FOR COST MANAGEMENT ***(10 Periods)***

Linear Programming, PERT/CPM, Transportation problems, Assignment problems, Learning Curve Theory.

Total Periods: 45

EXPERIENTIAL LEARNING

1 Prepare a mini-project report regarding cost control techniques in manufacturing units.
2 Prepare a report on real-life engineering project case studies, especially those that faced cost overruns or successfully managed costs
3 Conduct hands-on budgeting exercises where participants are given a project scope, and they have to create detailed budgets.

RESOURCES

TEXT BOOKS:

1. John M. Nicholas, Herman Steyn Project Management for Engineering, Business and Technology, Taylor & Francis, 2 August 2020, ISBN: 9781000092561
2. Albert Lester ,Project Management, Planning and Control, Elsevier/Butterworth-Heinemann, 2007, ISBN: 9780750669566, 075066956X.

REFERENCE BOOKS:

1. Charles T. Horngren et al Cost Accounting a Managerial Emphasis, Prentice Hall of India, New Delhi, 2011.
2. Ashish K. Bhattacharya, Principles & Practices of Cost Accounting A. H. Wheeler publisher, 1991.
3 Vohra N.D., Quantitative Techniques in Management, Tata McGraw Hill Book Co. Ltd, 2007
4 Robert S Kaplan Anthony A. Alkinson, Management & Cost Accounting, 2003

VIDEO LECTURES:

1. https://www.youtube.com/watch?v=rck3MnC7OXA
2. https://www.youtube.com/watch?v=QWD1LMzStI4

WEB RESOURCES:

1. https://www.superfastcpa.com/what-are-cost-concepts-in-decision-making
2. https://www.indeed.com/career-advice/career-development/project-cost-controls
3. https://www.geeksforgeeks.org/difference-between-pert-and-cpm/

UNIVERSITY ELECTIVE

Course Code	Course Title	L	T	P	S	C
22CE201701	**DISASTER MANAGEMENT**	3	-	-	-	3

Pre-Requisite -

Anti-Requisite -

Co-Requisite -

COURSE DESCRIPTION: This course provides a detailed discussion on disaster prone areas in India, repercussions of disasters and hazards, disaster preparedness and management, risk assessment and disaster management.

COURSE OUTCOMES: After successful completion of the course, students will be able to:

CO1. Analyze the vulnerability of an area to natural and man-made disasters/hazards as per the guidelines to solve complex problems using appropriate techniques ensuring safety, environment and sustainability.

CO2. Analyze the causes and impacts of disasters using appropriate tools and techniques and suggest mitigation measures ensuring safety, environment and sustainability besides communicating effectively in graphical form.

CO3. Suggest the preparedness measures using appropriate tools and techniques and suggest mitigation measures ensuring safety, environment and sustainability.

CO4. Analyze the Risk Assessment using appropriate tools and techniques and suggest mitigation measures ensuring safety, environment and sustainability.

CO5. Design disaster management strategies to solve pre, during and post disaster problems using appropriate tools and techniques following the relevant guidelines and latest developments ensuring safety, environment and sustainability besides communicating effectively in graphical form.

CO-PO Mapping Table:

Course Outcomes	Program Outcomes					
	PO1	PO2	PO3	PO4	PO5	PO6
CO1	-	-	-	-	-	2
CO2	-	-	-	-	-	2
CO3	-	-	-	-	-	2
CO4	-	-	-	-	-	2
CO5	-	-	-	-	-	2
Course Correlation Level	-	-	-	-	-	2

Correlation Levels: 3: High; 2: Medium; 1: Low

COURSE CONTENT

Module 1: DISASTER PRONE AREAS IN INDIA ***(09 Periods)***

Introduction: Disaster: Definition, Factors and Significance; Difference Between Hazard and Disaster; Natural and Manmade Disasters: Difference, Nature, Types And Magnitude. **Disaster Prone Areas:** Study Of Seismic Zones; Areas Prone To Floods And Droughts, Landslides And Avalanches; Areas Prone To Cyclonic And Coastal Hazards With Special Reference To Tsunami; Post-Disaster Diseases And Epidemics.

Module 2: REPERCUSSIONS OF DISASTERS AND HAZARDS ***(09 Periods)***

Economic Damage, Loss of Human and Animal Life, Destruction of Ecosystem. Natural Disasters: Earthquakes, Volcanisms, Cyclones, Tsunamis, Floods, Droughts And Famines, Landslides And Avalanches, Man-made disaster: Nuclear Reactor Meltdown, Industrial Accidents, Oil Slicks And Spills, Outbreaks Of Disease And Epidemics, War And Conflicts.

Module 3: DISASTER PREPAREDNESS AND MANAGEMENT ***(11 Periods)***

Preparedness: Monitoring Of Phenomena Triggering A Disaster Or Hazard; Evaluation Of Risk: Application Of Remote Sensing, Data From Meteorological And Other Agencies, Media Reports: Governmental And Community Preparedness.

Module 4: RISK ASSESSMENT ***(08 Periods)***

Disaster Risk: Concept and Elements, Disaster Risk Reduction, Global and National Disaster Risk Situation. Techniques of Risk Assessment, Global Co-Operation In Risk Assessment And Warning, People's Participation In Risk Assessment. Strategies for Survival.

Module 5: DISASTER MANAGEMENT ***(08 Periods)***

Disaster management organization and methodology, Disaster management cycle, Disaster management in India – Typical cases and Cost–benefit analysis, Disaster management programs implemented by NGOs and Government of India, Usage of GIS and Remote sensing techniques in disaster management, Leadership and Coordination in Disaster management, Emerging trends in disaster management.

Total Periods: 45

EXPERIENTIAL LEARNING

1. Perform hazard assessment and vulnerability analysis for any nearby town/city and prepare a detailed report of possible impacts of various disasters on environment, infrastructure and development.
2. Prepare a detailed report on the causes and effects of Tsunami that was occurred in the year 2004. Also discuss various advancements in Tsunami warning systems.
3. Identify the major causes of urban floods in cities like Chennai, Hyderabad & Mumbai. Also list various mitigation strategies to reduce the impact of floods.
4. Prepare a detailed report on how various man-made activities are directly/indirectly related to the occurrence of landslides that occurred in recent days in India.
5. Visit AP State Disaster Response and Fire Services Department and record about various methods used by them in mitigating disasters and their management.

RESOURCES

TEXT BOOKS:

1. Sharma V. K., *Disaster Management, Medtech Publishing, 2nd Edition, 2013*.
2. Anand S. Arya, Anup Karanth, and Ankush Agarwal, *Hazards, Disasters and Your Community: A Primer for Parliamentarians*, GOI–UNDP Disaster Risk Management Programme, Government of India, National Disaster Management Division, Ministry of Home Affairs, New Delhi, Version 1.0, 2005

REFERENCE BOOKS:

1. Donald Hyndman and David Hyndman, *Natural Hazards and Disasters*, Cengage Learning, USA, 5th Edition, 2015.
2. *Disaster Management in India,* A Status Report, Ministry of Home Affairs, Govt. of India, May 2011.
3. Rajendra Kumar Bhandari, *Disaster Education and Management: A Joyride for Students, Teachers, and Disaster Managers*, Springer India, 2014.
4. Singh R. B., *Natural Hazards and Disaster Management*, Rawat Publications, 2009.
5. R. Nishith, Singh AK, *Disaster Management in India: Perspectives, issues and strategies,* New Royal book Company.
6. Sahni, PardeepEt.Al. (Eds.), *Disaster Mitigation Experiences And Reflections*, Prentice Hall of India, New Delhi.
7. Goel S. L. , *Disaster Administration And Management Text And Case Studies*, Deep &Deep Publication Pvt. Ltd., New Delhi

VIDEO LECTURES:

1. https://nptel.ac.in/courses/105104183
2. https://www.digimat.in/nptel/courses/video/124107010/L01.html

Web Resources:

1. https://egyankosh.ac.in/handle/123456789/25093
2. https://www.egyankosh.ac.in/handle/123456789/25912
3. https://www.nios.ac.in/media/documents/333courseE/12.pdf
4. https://ndmindia.mha.gov.in/images/public-awareness/Primer%20for%20Parliamentarians.pdf

UNIVERSITY ELECTIVE

Course Code	Course Title	L	T	P	S	C
22SS201701	**VALUE EDUCATION**	3	-	-	-	3

Pre-Requisite -

Anti-Requisite -

Co-Requisite -

COURSE DESCRIPTION: This course deals with understanding the value of education and self-development, Imbibe good values in students, and making them know about the importance of character.

COURSE OUTCOMES: After successful completion of the course, students will be able to:

CO1. Demonstrate the knowledge of values and self-development
CO2. Analyze the importance of the cultivation of values.
CO3. Learn suitable aspects of personality and behavioral development
CO4. Function as a member and leader in multi-disciplinary teams by avoiding faulty thinking.
CO5. Develop character and competence for effective studies.

CO-PO Mapping Table:

Course Outcomes	Program Outcomes					
	PO1	PO2	PO3	PO4	PO5	PO6
CO1	-	-	-	-	-	2
CO2	-	-	-	-	-	2
CO3	-	-	-	-	-	2
CO4	-	-	-	-	-	2
CO5	-	-	-	-	-	2
Course Correlation Level	-	-	-	-	-	2

Correlation Levels: 3: High; 2: Medium; 1: Low

COURSE CONTENT

Module 1: VALUES AND SELF-DEVELOPMENT ***(09 Periods)***

Values and self-development –Social values and individual attitudes. Work ethics, Indian vision of humanism. Moral and non-moral valuation. Standards and principles. Value judgements- Case studies

Module 2: IMPORTANCE OF CULTIVATION OF VALUES. ***(09 Periods)***

Importance of cultivation of values. Sense of duty. Devotion, Self-reliance. Confidence, Concentration. Truthfulness, Cleanliness. Honesty, Humanity. Power of faith, National Unity. Patriotism. Love for nature, Discipline- Case studies

Module 3: PERSONALITY AND BEHAVIOR DEVELOPMENT ***(09 Periods)***

Personality and Behavior Development - Soul and Scientific attitude. Positive Thinking. Integrity and discipline, Punctuality, Love and Kindness - Case studies

Module 4: AVOID FAULTY THINKING. ***(09 Periods)***

Avoid fault Thinking. Free from anger, Dignity of labour. Universal brotherhood and religious tolerance. True friendship. Happiness Vs suffering, love for truth. Aware of self-destructive habits. Association and Cooperation. Doing best for saving nature - Case studies

Module 5: CHARACTER AND COMPETENCE ***(09 Periods)***

Character and Competence –Holy books vs Blind faith. Self-management and Good health. Science of reincarnation, Equality, Nonviolence, Humility, Role of Women. All religions and the same message. Mind your Mind, Self-control. Honesty, Studying effectively- Case studies

Total Periods: 45

EXPERIENTIAL LEARNING

1. Demonstrate orally using your experiences of what values are naturally acceptable in a relationship to nurture or exploit others.
2. Prepare a report by identifying and analyzing the importance of cultivation of values.
3. Present a poster on different attitudes and behaviours.
4. Students give a PowerPoint presentation on doing best for nature.
5. Students are encouraged to bring a daily newspaper to class or to access any news related to the need for human values and note down the points.
6. Prepare a case study on how to maintain harmony with different religious people through character and competence.

(It’s an indicative one. The Course Instructor may change the activities and the same shall be reflected in the Course Handout)

RESOURCES

TEXTBOOKS:

1. R. Subramanaian, *Professional Ethics*, Oxford Higher Education, 2013.
2. Mike W. Martin and Roland Schinzinger, *Ethics in Engineering*, Tata McGraw-Hill, 3rd Edition 2007.
3. Chakravarthy, S.K.: Values and ethics for Organizations: Theory and Practice, Oxford University Press, NewDelhi, 1999.

REFERENCE BOOKS:

1. M.G. Chitakra: Education and Human Values, A.P.H. Publishing Corporation, New Delhi, 2003
2. Awakening Indians to India, Chinmayananda Mission, 2003
3. Satchidananda, M.K.: Ethics, Education, Indian Unity and Culture, Ajantha Publications, Delhi, 1991

VIDEO LECTURES:

1. https://www.youtube.com/watch?v=90VQPZURN5c
2. https://www.youtube.com/watch?v=6ofPcK0uDaA
3. https://www.youtube.com/watch?v=5_f-7zCi79A
4. https://www.youtube.com/watch?v=2ve49BWAJRE
5. https://www.youtube.com/watch?v=kCOIfnxxQ5U

WEB RESOURCES:

1. https://www.livingvalues.net/
2. https://livingvalues.net/materials-for-schools/
3. https://www.edb.gov.hk/en/curriculum-development/4-key-tasks/moral-civic/index.html

UNIVERSITY ELECTIVE

Course Code	Course Title	L	T	P	S	C
22SS201702	**PEDAGOGY STUDIES**	3	-	-	-	3

Pre-Requisite -

Anti-Requisite -

Co-Requisite -

COURSE DESCRIPTION: This course deals with understanding pedagogical practices that are being used by teachers in formal and informal classrooms, the effectiveness of pedagogical practices, teacher education (curriculum and practicum), and the school curriculum and guidance materials that can best support effective pedagogy.

COURSE OUTCOMES: After successful completion of the course, students will be able to:

CO1 Demonstrate knowledge of pedagogical methodology
CO2 Analyze the functional knowledge in Pedagogical practices, Curriculum, and Teacher Education
CO3 Learn effective pedagogical practices and apply strategies.
CO4 Function effectively as an individual and as a member of the Professional development.
CO5 Understand research Gaps and provide future Directions.

CO-PO Mapping Table:

Course Outcomes	Program Outcomes					
	PO1	PO2	PO3	PO4	PO5	PO6
CO1	-	-	-	-	-	2
CO2	-	-	-	-	-	2
CO3	-	-	-	-	-	2
CO4	-	-	-	-	-	2
CO5	-	-	-	-	-	2
Course Correlation Level	-	-	-	-	-	2

Correlation Levels: 3: High; 2: Medium; 1: Low

COURSE CONTENT

Module 1: INTRODUCTION AND METHODOLOGY *(09 Periods)*

Aims and rationale, Policy background, Conceptual framework and terminology Theories of learning, Curriculum, Teacher education. Conceptual framework, Research questions. Overview of Methodology and Searching- Case studies

Module 2: THEMATIC OVERVIEW *(09 Periods)*

Pedagogical practices are being used by teachers in formal and informal classrooms in developing countries. Curriculum, Teacher Education- Case studies

Module 3: EFFECTIVENESS OF PEDAGOGICAL PRACTICES *(09 Periods)*

Evidence on the effectiveness of pedagogical practices, Methodology for the in-depth stage: quality assessment of included studies, teacher education (curriculum and practicum) and the school curriculum and guidance materials best support effective pedagogy, Theory of change, Strength and nature of the body of evidence for effective pedagogical practices. Pedagogic theory and pedagogical approaches. Teachers' Attitudes and beliefs and Pedagogic strategies- Case studies

Module 4: PROFESSIONAL DEVELOPMENT *(09 Periods)*

alignment with classroom practices and follow-up support, Peer support, and Support from the head teacher and the community. Curriculum and assessment, Barriers to learning: limited resources and large class sizes- Case studies

Module 5: RESEARCH GAPS AND FUTURE DIRECTIONS *(09 Periods)*

Research design, Contexts, Pedagogy, Teacher Education, Curriculum and Assessment, Dissemination and research impact- Case studies

Total Periods: 45

EXPERIENTIAL LEARNING

1. List out the self-improvement in you after going through pedagogical methodologies.
2. Discuss different practices that you would like to adopt in the curriculum.
3. Describe in your own words how can you bring effectiveness to the curriculum.
4. Imagine you are a head teacher and illustrate different barriers to learning.
5. Assume you are a teacher and Interpret different directions that you would bring for the assessment of the students.

(It's an indicative one. The Course Instructor may change the activities and the same shall be reflected in the Course Handout)

RESOURCES

TEXTBOOK:

1. Ackers J, Hardman F (2001) Classroom interaction in Kenyan primary schools, Compare, 31 (2): 245-261.
2. Alexander RJ (2001) Culture and pedagogy: International comparisons in primary education.

REFERENCES:

1. Akyeampong K (2003) Teacher training in Ghana - does it count? Multi-site teacher education
2. Agrawal M (2004) Curricular reform in schools: The importance of evaluation, Journal of Curriculum Studies, 36 (3): 361-379.Oxford and Boston: Blackwell.
3. Akyeampong K, Lussier K, Pryor J, Westbrook J (2013) Improving teaching and learning of basic maths and reading in Africa: Does teacher preparation count? International Journal Educational Development, 33 (3): 272–282.
4. Chavan M (2003) Read India: A mass scale, rapid, 'learning to read' campaign.

VIDEO LECTURES:

1. https://www.youtube.com/watch?v=WL40UeySag4
2. https://www.youtube.com/watch?v=MMXaXDIHFJ8
3. https://www.youtube.com/watch?v=7uJL1R6M4Iw

WEB RESOURCES:

1. https://acrl.ala.org/IS/instruction-tools-resources-2/pedagogy/a-selected-list-of-journals-on-teaching-learning/
2. https://guides.douglascollege.ca/TLonline/resourcesforonlinepedagogy
3. https://www.refseek.com/directory/teacher_resources.html

UNIVERSITY ELECTIVE

Course Code	Course Title	L	T	P	S	C
22LG201701	PERSONALITY DEVELOPMENT THROUGH LIFE ENLIGHTENMENT SKILLS	3	-	-	-	3

Pre-Requisite -

Anti-Requisite -

Co-Requisite -

COURSE DESCRIPTION: This course gives awareness to students about the various dynamics of personality development.

COURSE OUTCOMES: After successful completion of the course, students will be able to:

CO1. Demonstrate knowledge in Self-Management and Planning Career

CO2. Analyze the functional knowledge in attitudes and thinking strategies

CO3. Learn and apply soft skills for professional success.

CO4. Function effectively as an individual and as a member in diverse teams

CO5. Communicate effectively in public speaking in formal and informal situations.

CO-PO Mapping Table:

Course Outcomes	Program Outcomes					
	PO1	PO2	PO3	PO4	PO5	PO6
CO1	-	-	-	-	-	2
CO2	-	-	-	-	-	2
CO3	-	-	-	-	-	2
CO4	-	-	-	-	-	2
CO5	-	-	-	-	-	2
Course Correlation Level	-	-	-	-	-	2

Correlation Levels: 3: High; 2: Medium; 1: Low

COURSE CONTENT

Module 1: SELF-ESTEEM & SELF-IMPROVEMENT *(09 Periods)*

Know Yourself – Accept Yourself; Self-Improvement: Plan to Improve - Actively Working to Improve Yourself- Exercises- case studies

Module 2: DEVELOPING POSITIVE ATTITUDES *(09 Periods)*

How Attitudes Develop – Attitudes are Catching – Improve Your Attitudes – Exercises- case studies

Module 3 SELF-MOTIVATION & SELF-MANAGEMENT *(09 Periods)*

Show Initiative – Be Responsible Self-Management; Efficient Work Habits – Stress Management – Employers Want People Who can Think – Thinking Strategies- Exercises- case studies

Module 4 GETTING ALONG WITH THE SUPERVISOR *(09 Periods)*

Know your Supervisor – Communicating with your Supervisor – Special Communication with your Supervisor – What Should you Expect of Your Supervisor? – What your Supervisor expects of you - Moving Ahead Getting Along with your Supervisor- Exercises- case studies

Module 5 WORKPLACE SUCCESS *(09 Periods)*

First Day on the Job – Keeping Your Job – Planning Your Career – Moving Ahead- Exercises- case studies

Total Periods: 45

EXPERIENTIAL LEARNING

1. List out the self-improvements in you on the charts and explain in detail.
2. Discuss different famous personalities and their attitudes.
3. Describe different personalities with respect to self-motivation and self-management.
4. Imagine you are a supervisor and illustrate different special communications.
5. Assume and Interpret different experiences on the first day of your job.

RESOURCES

TEXTBOOK:

1 Harold R. Wallace and L. Ann Masters, Personal Development for Life and Work, Cengage Learning, Delhi, 10th edition Indian Reprint, 2011. (6th Indian Reprint 2015)

2 Barun K. Mitra, Personality Development and Soft Skills, Oxford University Press, 2011.

REFERENCE BOOKS:

1. K. Alex, Soft Skills, S. Chand & Company Ltd, New Delhi, 2nd Revised Edition, 2011.
2. Stephen P. Robbins and Timothy A. Judge, Organizational Behaviour, Prentice Hall, Delhi, 16th edition, 2014

VIDEO LECTURES:

1. https://www.youtube.com/watch?v=6Y5VWBLi1es
2. https://www.youtube.com/watch?v=H9qA3inVMrA

Web Resources:

1. https://www.universalclass.com/.../the-process-of-perso...
2. https://www.ncbi.nlm.nih.gov/pubmed/25545842
3. https://www.youtube.com/watch?v=Tuw8hxrFBH8